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# Agassi

DTX

FAB-B

## CPU:

Intel Lynnfield/Havendale processors in LGA1156 Package

## System Chipset:

PCH(Ibex Peak)

## Main Memory:

Dual Channel / DDR-III \* 4 (Max 16GB)

## On Board Device:

Clock Generator ICS9LRS4105

Super I/O:ITE8721F-CX

LAN:RTL8111E

HDA Codec:ALC662

BIOS:SPI Flash ROM(32MX2)

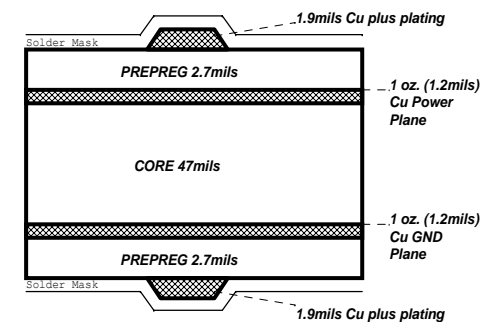
## Expansion Slots:

PCI EXPRESS 16X SLOT \* 1

PCI EXPRESS 1X SLOT \* 1

## Board Stack-up

(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4-mil trace target, ±15%

USB2.0	- 90	ohm : 17.5%
SATA	- 90	ohm : 17.5%
PCIE1.1	- 80	ohm : 17.5%
DMI	- 80	ohm : 17.5%
PCIE2.0	- 80	ohm : 17.5%
HDMI	- 95	ohm : 17.5%

Version	Function	SKU	BOM
Fab.A			
Fab.B			

**FOXCONN®**

**FOXCONN PCEG**

Title

**Cover Sheet**

Size  
A3

Document Number

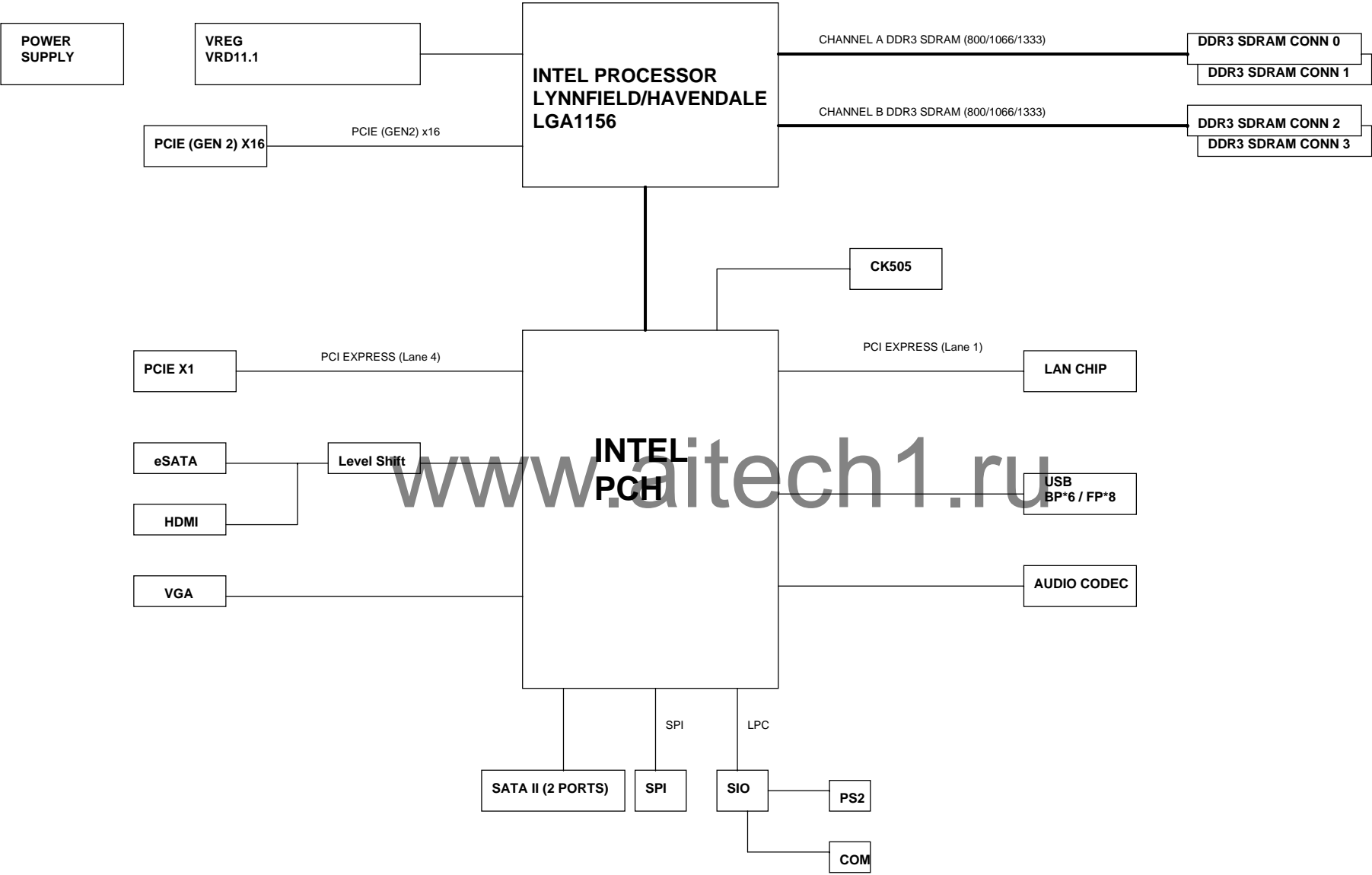
**Agassi**

Rev  
1.0

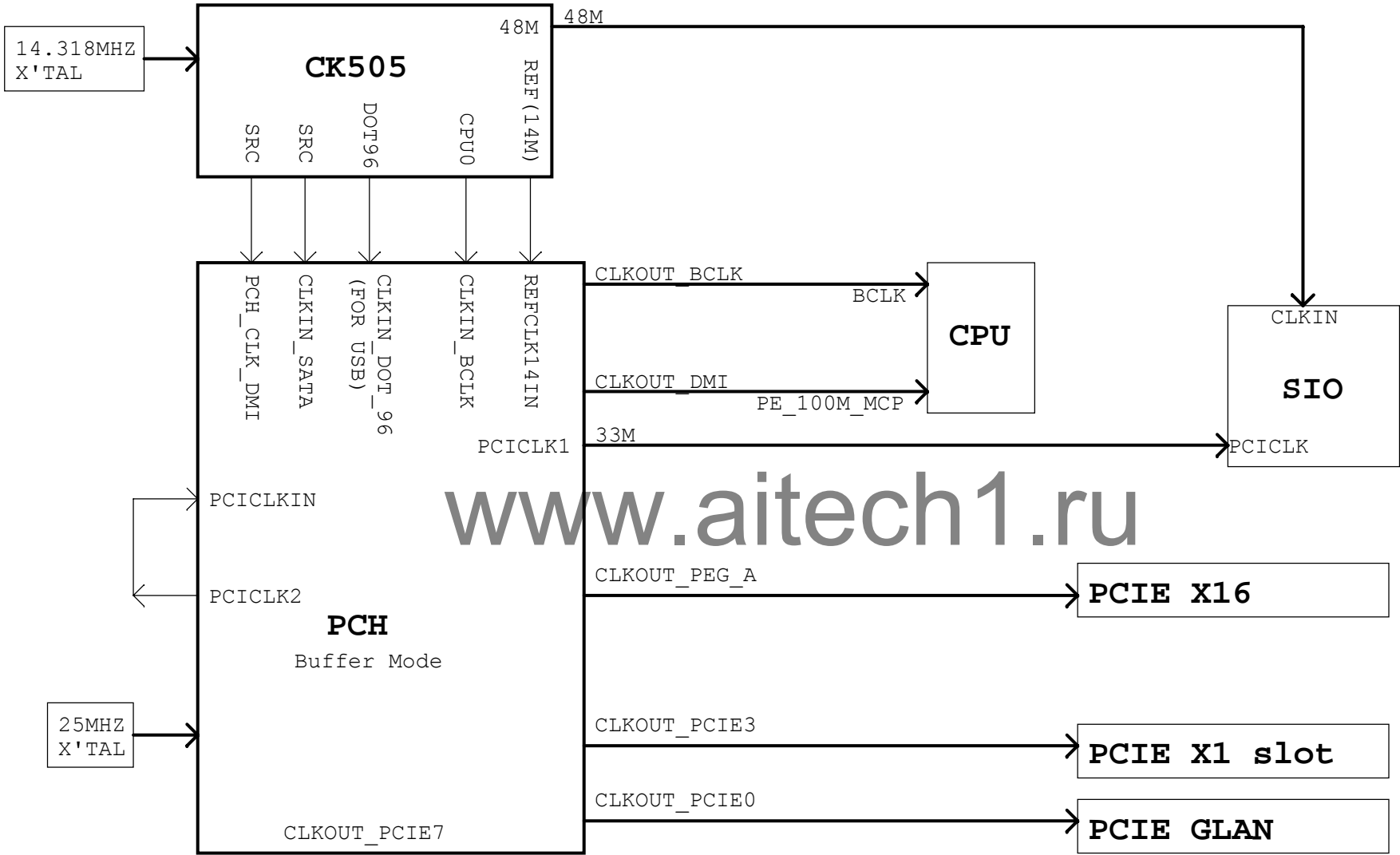
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BLOCK DIAGRAM



CLOCK DISTRIBUTION



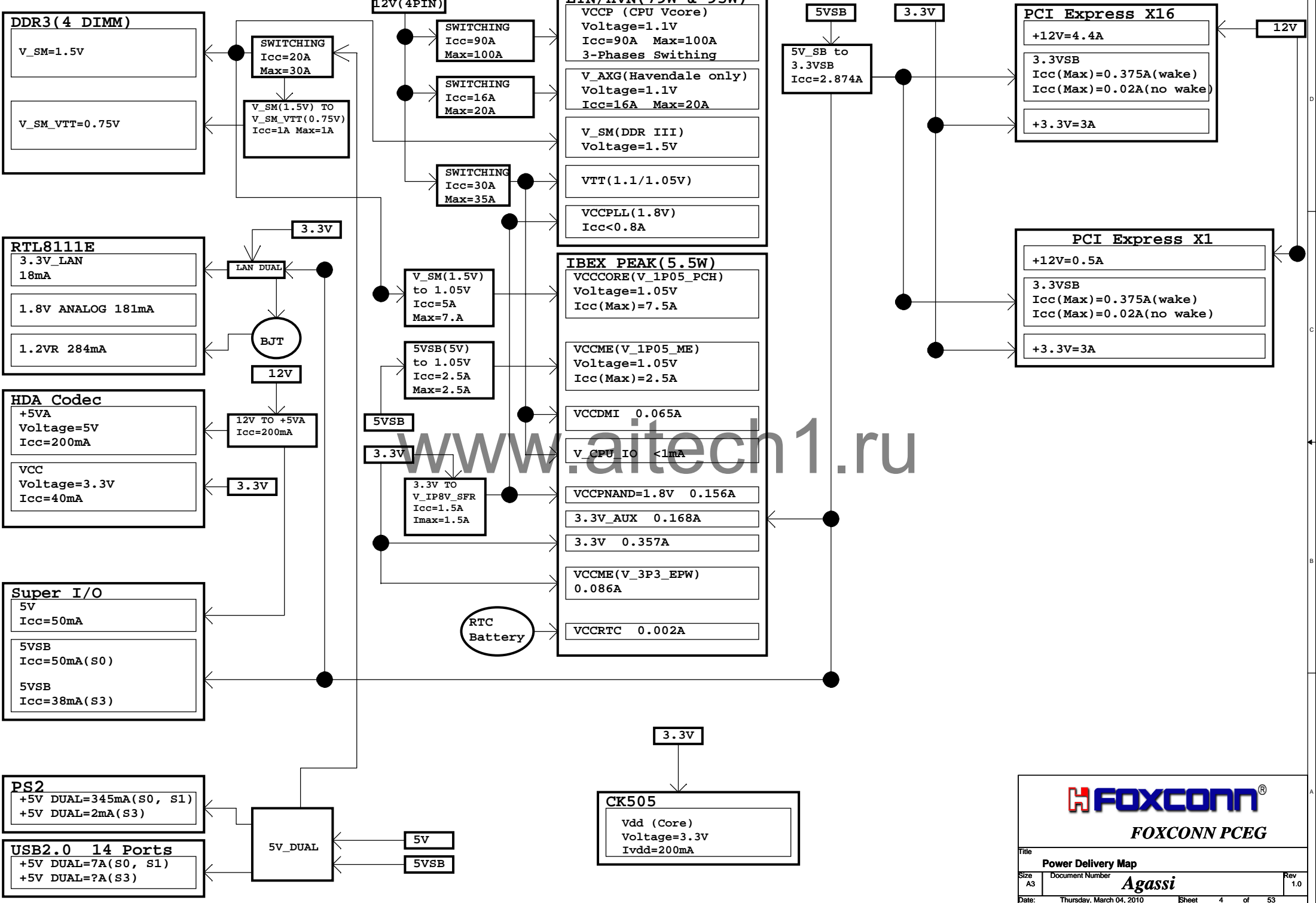
www.aitech1.ru



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Title			Clock Distribution		
Size	A3	Document Number	Agassi		
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POWER DELIVERY MAP



POWER ON SEQUENCE

Figure 8-1. G3 w/RTC Loss to S4/S5 Timing Diagram

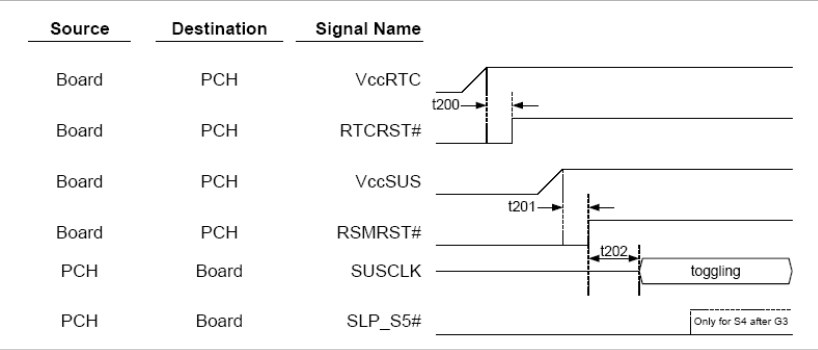


Figure 8-3. S3/M3 to S0 Timing Diagram

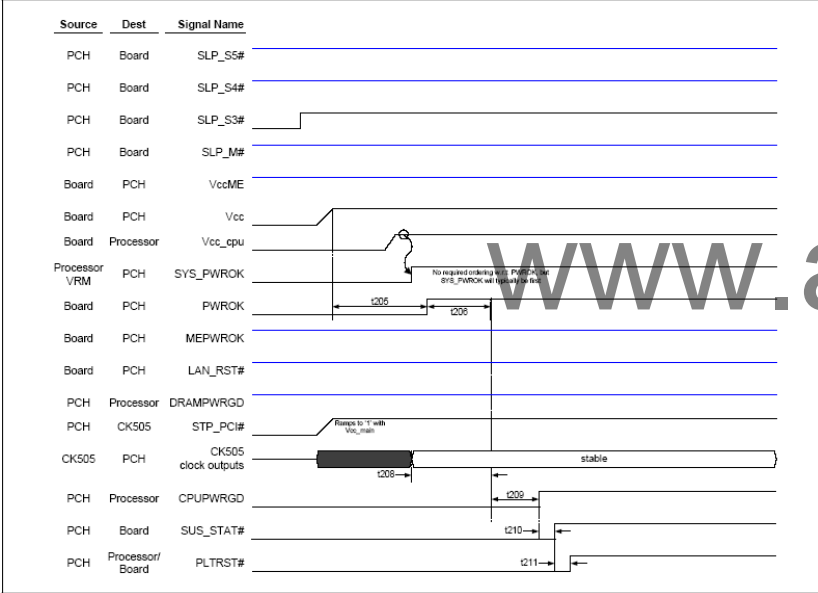


Figure 8-6. DRAMPWRGD Timing Diagram

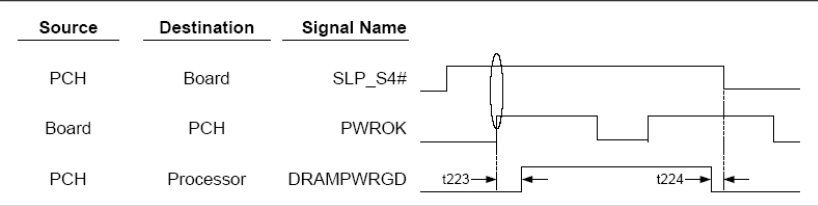


Figure 8-2. S5 to S0 Timing Diagram

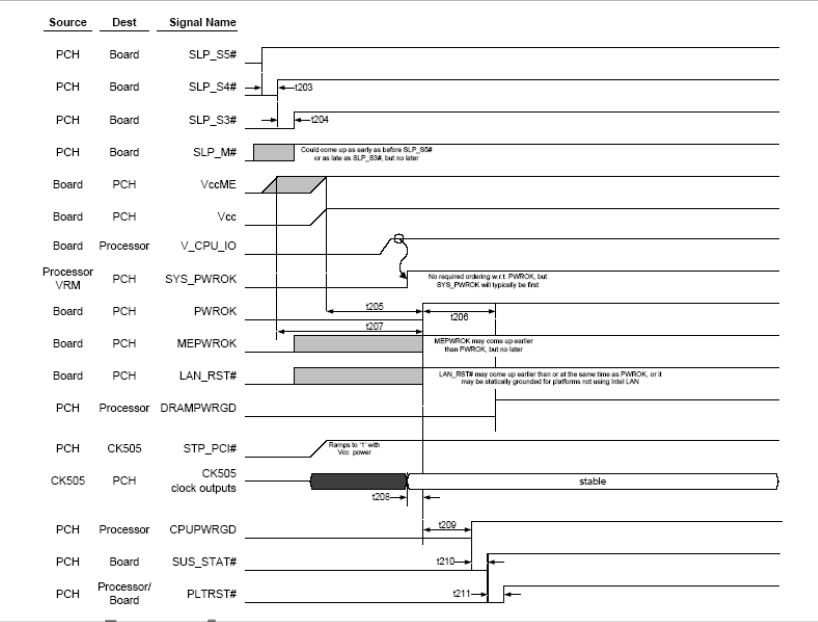
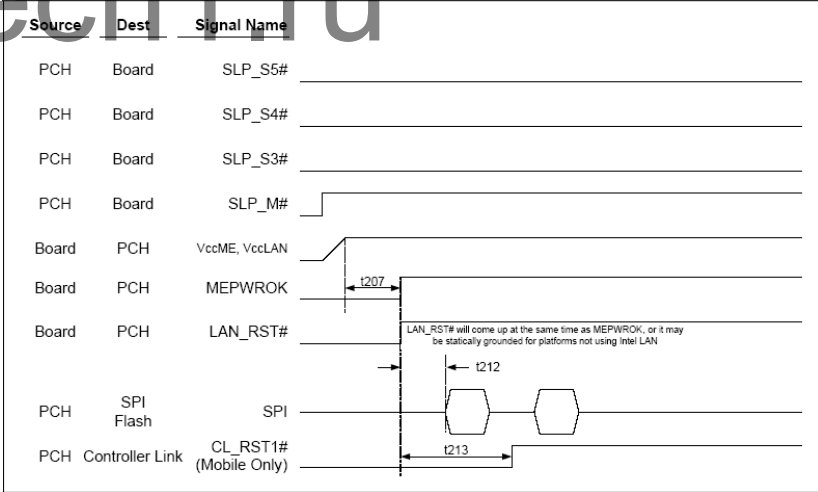
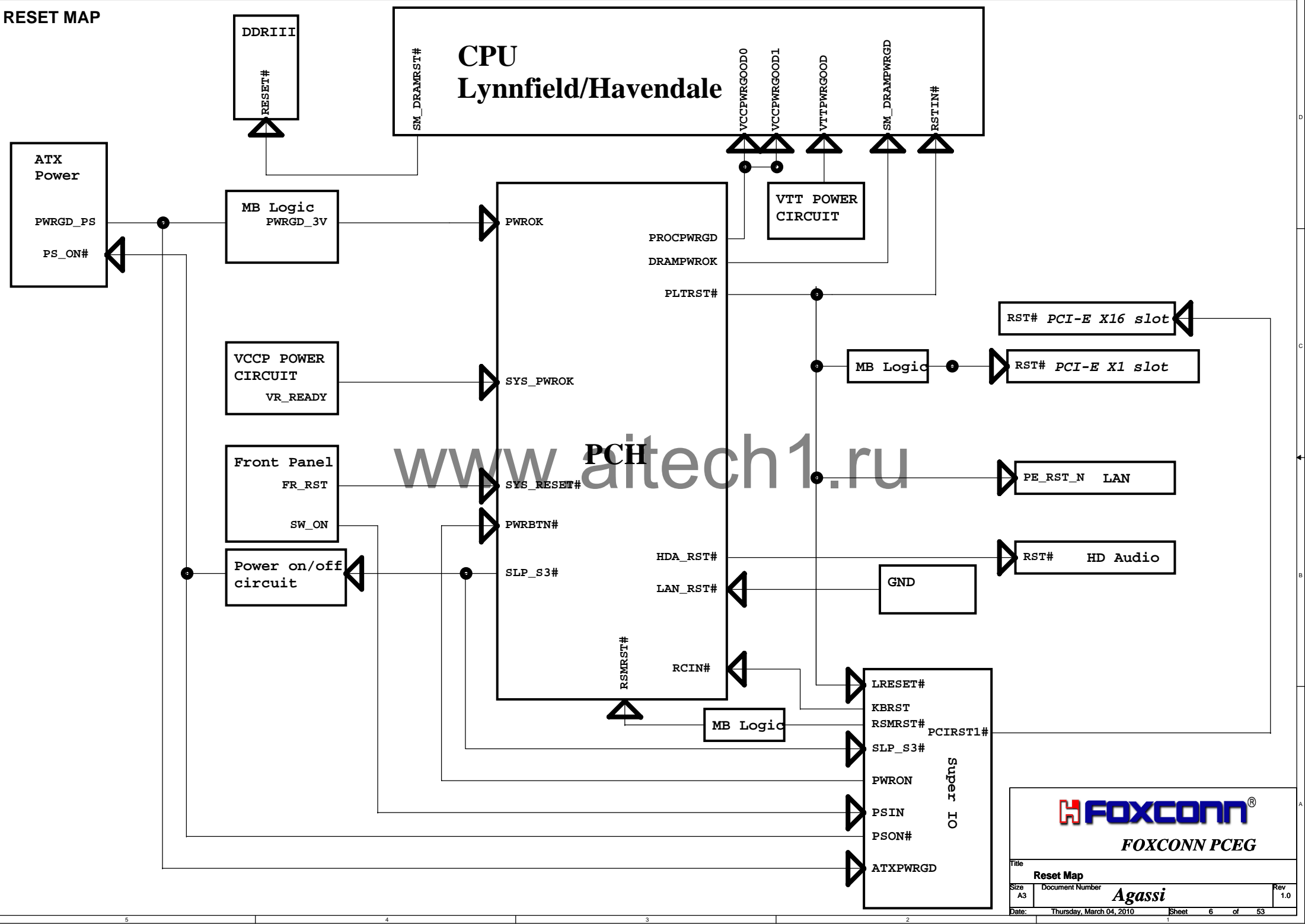


Figure 8-4. S5/Moff - S5/M3 Timing Diagram




RESET MAP



PCH GPIO TABLE	
PIN NAME	FUNCTION
REQ1#/GPIO50	K_PCI_REQ#1(not used) Pull up to 3.3V
GNT1#/GPIO51	Not connect
REQ2#/GPIO52	K_PCI_REQ#2(not used) Pull up to 3.3V
GNT2#/GPIO53	Not connect
REQ3#/GPIO54	K_PCI_REQ#3(not used) Pull up to 3.3V
PIRQ5#/GPIO55	Not connect
PIRQ6#/GPIO56	K_PCI_INT_E#(not used) Pull up to 3.3V
PIRQF#/GPIO57	K_PCI_INT_F#(not used) Pull up to 3.3V
PIRQG#/GPIO58	K_PCI_INT_G#(not used) Pull up to 3.3V
PIRQH#/GPIO59	THERMAL_SHUTDOWN, Pull up to 3.3V
OC0#/GPIO59	U_USB_OC_R_#0
OC1#/GPIO40	U_USB_OC_R_#1
OC2#/GPIO41	U_USB_OC_R_#2
OC3#/GPIO42	U_USB_OC_R_#3
OC4#/GPIO43	U_USB_OC_R_#4
OC5#/GPIO9	U_USB_OC_R_#5
OC6#/GPIO10	U_USB_OC_R_#6
OC7#/GPIO14	U_USB_OC_R_#7
TACH0/GPIO17	S_PCH_CPU_FAN_TACH
TACH1/GPIO1	S_PCH_SYS_FAN_TACH1
TACH2/GPIO6	Pull up to 3.3V
TACH3/GPIO7	Pull up to 3.3V
SCLOCK/GPIO22	S_PCH_CONFIG_JUMPER(no used)PULL UP TO 1P05_PCH
SDATAOUT0/GPIO39	S_CRB_DETECT_GP39(no used) PULL UP TO 1P05_PCH
SDATAOUT1/GPIO48	S_SV_ADVANCE_GP48(no used) PULL UP TO 1P05_PCH
SLOAD/GPIO38	S_GP38_MFG_MODE#(no used) PULL UP TO 1P05_PCH
SATA0GP/GPIO21	S_SATA0GP PULL UP TO 3.3V
SATA1GP/GPIO19	S_SATA1GP PULL UP TO 3.3V
SATA2GP/GPIO36	S_CDC_DWN_DISABLE(no used)PULL UP TO 3.3V
SATA3GP/GPIO37	MCR (not used) Pull up to 3.3V
SATA4GP/GPIO16	H_SKT0CC_R_#
SATA5GP/GPIO49	S_PCH_GP49_PU PULL UP TO 3.3V
LDRQ1#/GPIO23	Not connect
SMBALERT#/GPIO11	S_SMBALERT# PULL UP TO 3.3V_AUX
SML0ALERT#/GPIO60	S_SML0ALERT PULL UP TO 3.3V_AUX
SML1ALERT#/GPIO74	S_SML1ALERT PULL UP TO 3.3V_AUX
SML1CLK/GPIO58	PULL UP TO 3.3V_AUX
SML1DATA/GP75	PULL UP TO 3.3V_AUX
BMBUSY#/GPIO0	A_FP_AUDIO_PRESENCE#
GPI08	S_IGC_EN#
SLP_LAN#/GPIO29	SLP_LAN#
SUS_PWR_ACK/GPIO30	S_SUS_PWR_ACK PULL UP TO 3.3V_AUX
LAN_PHY_PWR_CTRL/GPIO12	LAN_DISABLE#
GPI013	O_IO_PME#
GPI015	S_PCH_GP15 PULL UP TO 3.3V_AUX
PCICLKRQ1#/GPIO18	S_PCH_GP18_PU PULL UP TO 3.3V
PCICLKRQ2#/GPIO20	S_PCH_GP20_PU PULL UP TO 3.3V
MEM_LED/GPIO24	GPI0_YLW_HDR, Pull up to 3.3V_AUX
PCICLKRQ3#/GPIO25	S_1_WAIT1_CTRL_1, Pull up to 3.3V_AUX
PCICLKRQ4#/GPIO26	S_GP26_44_45_56_PD (no used), Pull up to 3.3V_AUX
GPI027	S_PCH_GP27 Pull up to 3.3V_AUX
GPI028	S_PCH_GP28_PU16r_XDP) PULL UP TO 3.3V_AUX
ADPRESENT/GPIO31	S_GP31_PU PULL UP TO 3.3V_AUX
GPI032	not used (TP162)
GPI033	S_ME_ENABLE
STP_PCI#/GPIO34	S_GP34_PU PULL UP TO 3.3V
SATACLKREQ#/GPIO35	Not used (TP78)
PCICLKRQ5#/GPIO44	S_GP26_44_45_56_PD (no used) Pull up to 3.3V_AUX
PCICLKRQ6#/GPIO45	S_GP26_44_45_56_PD (no used) Pull up to 3.3V_AUX
PCICLKRQ7#/GPIO46	S_GP46_47_PD PULL UP TO 3.3V_AUX
PEG_A_CLKRQ#/GPIO47	S_GP46_47_PD PULL UP TO 3.3V_AUX
PEG_B_CLKRQ#/GPIO56	S_GP26_44_45_56_PD (no used) Pull up to 3.3V_AUX
GPI057	TPM_PHY_PRESENT(no used) Pull Low
PCICLKRQ0#/GPIO73	SPI_WP_GPIO73 PULL UP TO 3.3_AUX
SUS_ATAT#/GPIO61	RF_KILLJ, Pull up to 3.3V_AUX
SUSCLK/GPIO62	TP65
SLP_SS#/GPIO63	S_SLP_SS#
GPI072	S_1_WAIT1_CTRL_2, Pull up to 3.3V_AUX
CLKOUTFLEX0/GPIO64	TP125
CLKOUTFLEX1/GPIO65	TP8
CLKOUTFLEX2/GPIO66	TP7
CLKOUTFLEX3/GPIO67	TP5

SIO GPIO TABLE	
PIN NAME	FUNCTION
PSON#/GP42	PS_ON#
PANSW/H#/GP43	PWRBTN#_SIO
PWRON#/GP44	S_PWRBTN#
RSMRST#/CIRR/XP55	SIO_RSMRST#
PWR0K1/GP13	SIO_PWRGD
PWR0K2/GP41	R_GPIO1 Pull up to 3.3VAUX
IRRX/GP46	R_GPIO2 Pull up to 3.3VAUX
VID06/GP17/R12#	SIO_BEEP
KRST#/GP62	KBRST# Pull up to 3.3V
KDAT/GP61	KBDATA
KCLK/GP60	KBCLK
MDAT/GP57	MSDATA
MCLK/GP56	MSCLK
VIN3/ATXPG	ATX_PWRGD
VID5/GP35	THERMAL_SHUTDOWN

SIO HW MONITOR	
PIN NAME	FUNCTION
VIN0	VIN0_VCCP
VIN1	VIN1_1P1_VTT
VIN2	VIN2_3D3V_SYS
VIN4	VIN4_+12V_SYS
VIN5	VIN5_5V_SYS
VIN6	VIN6_5VSB_SYS
TMPIN1	TMPIN1



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Title

**GPIO/IRQ/DSEL Table**

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Date:

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Sheet

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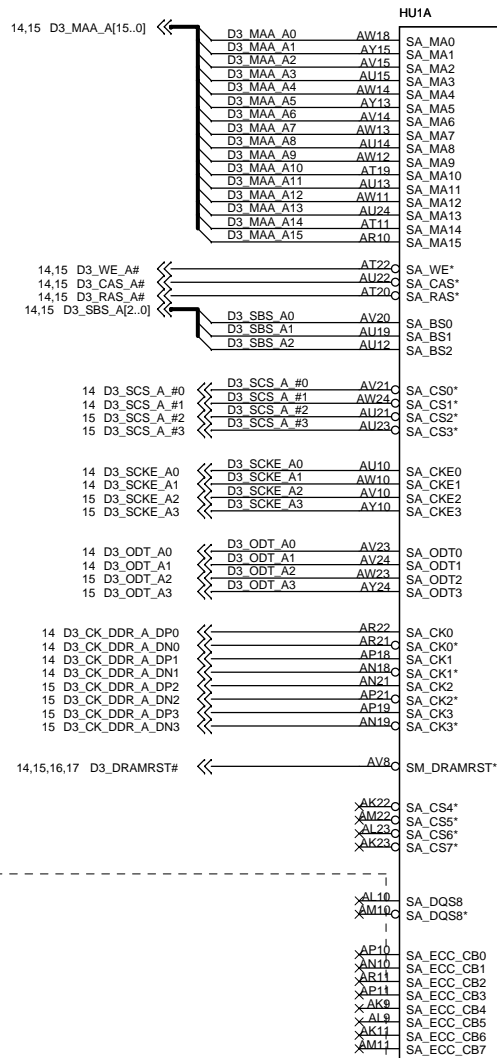
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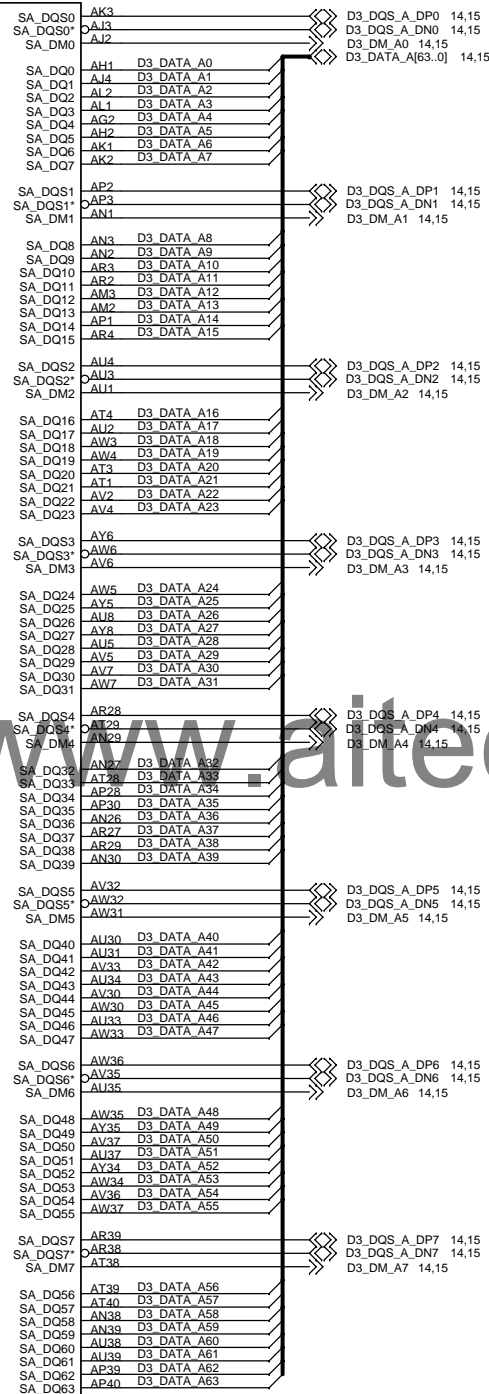




DDR\_A

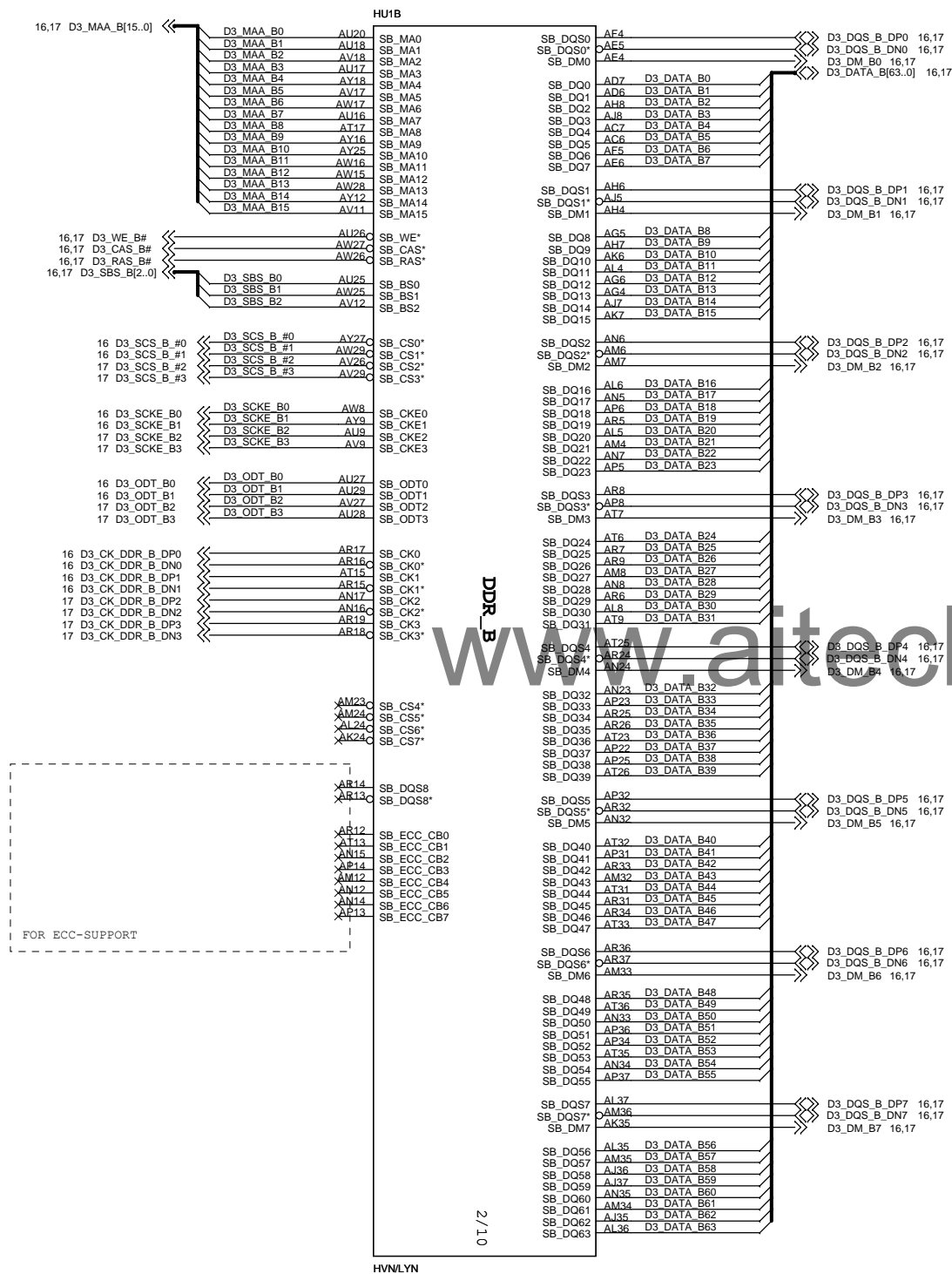
1 / 10

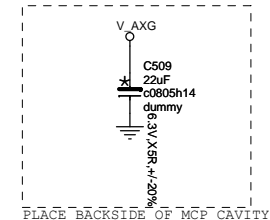
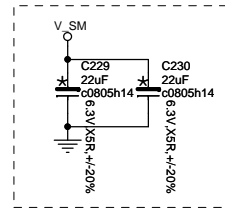
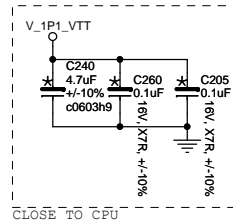
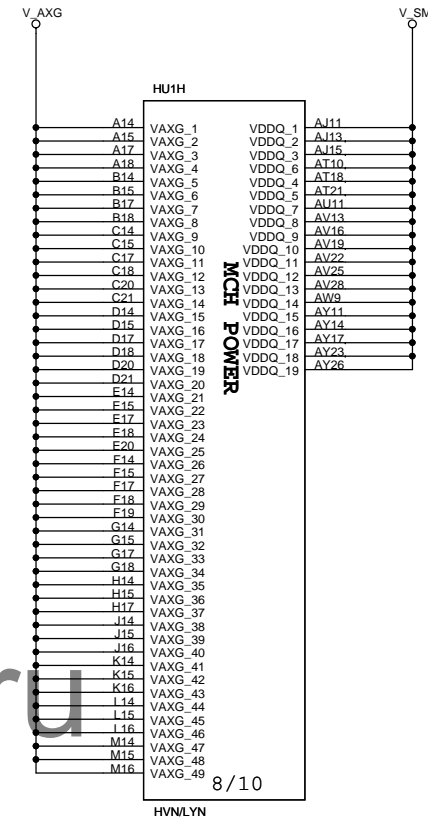
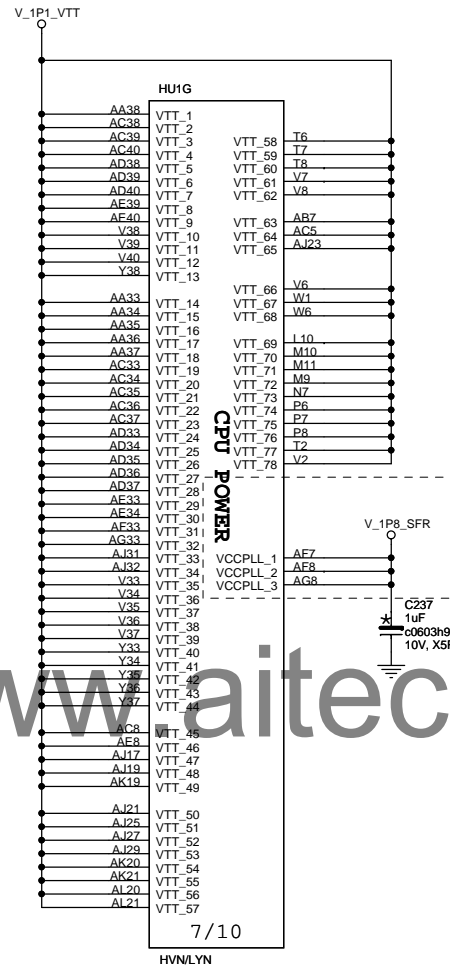
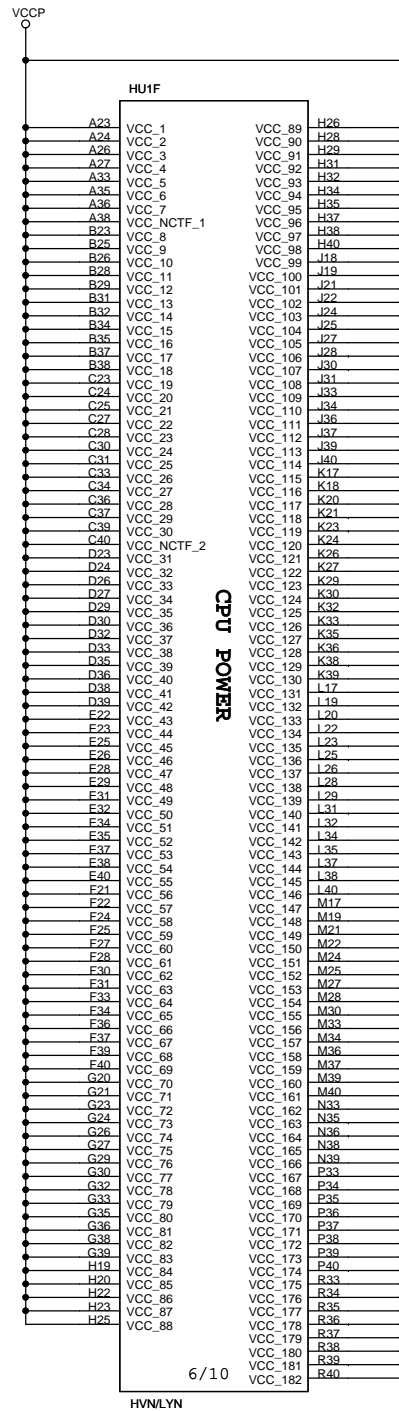
HVN/LYN



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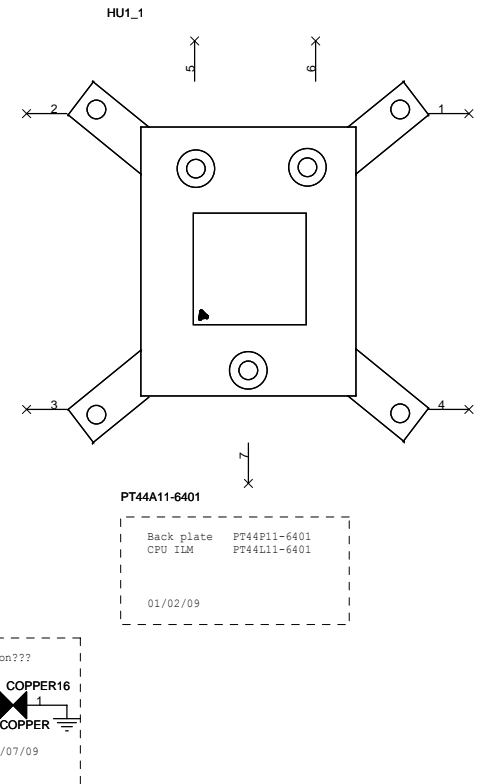
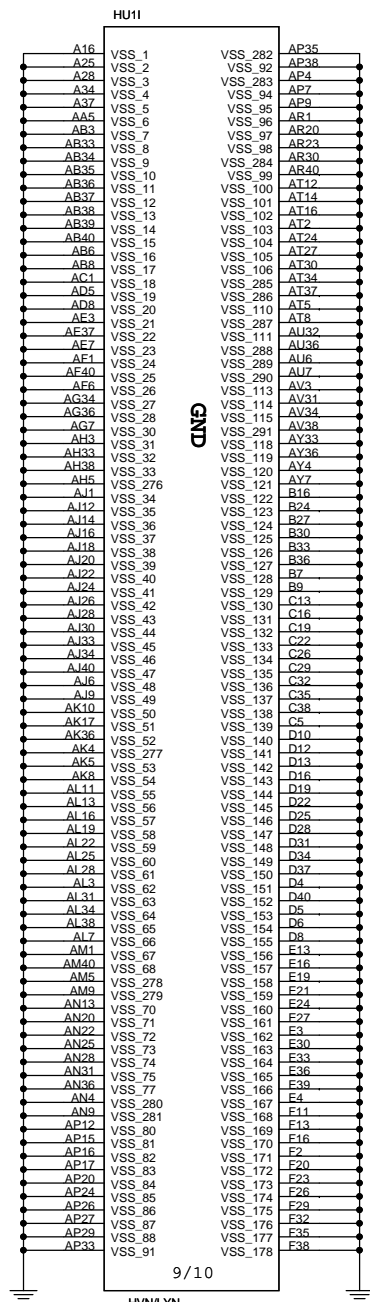
Title		CPU-3:DDR3_CHA
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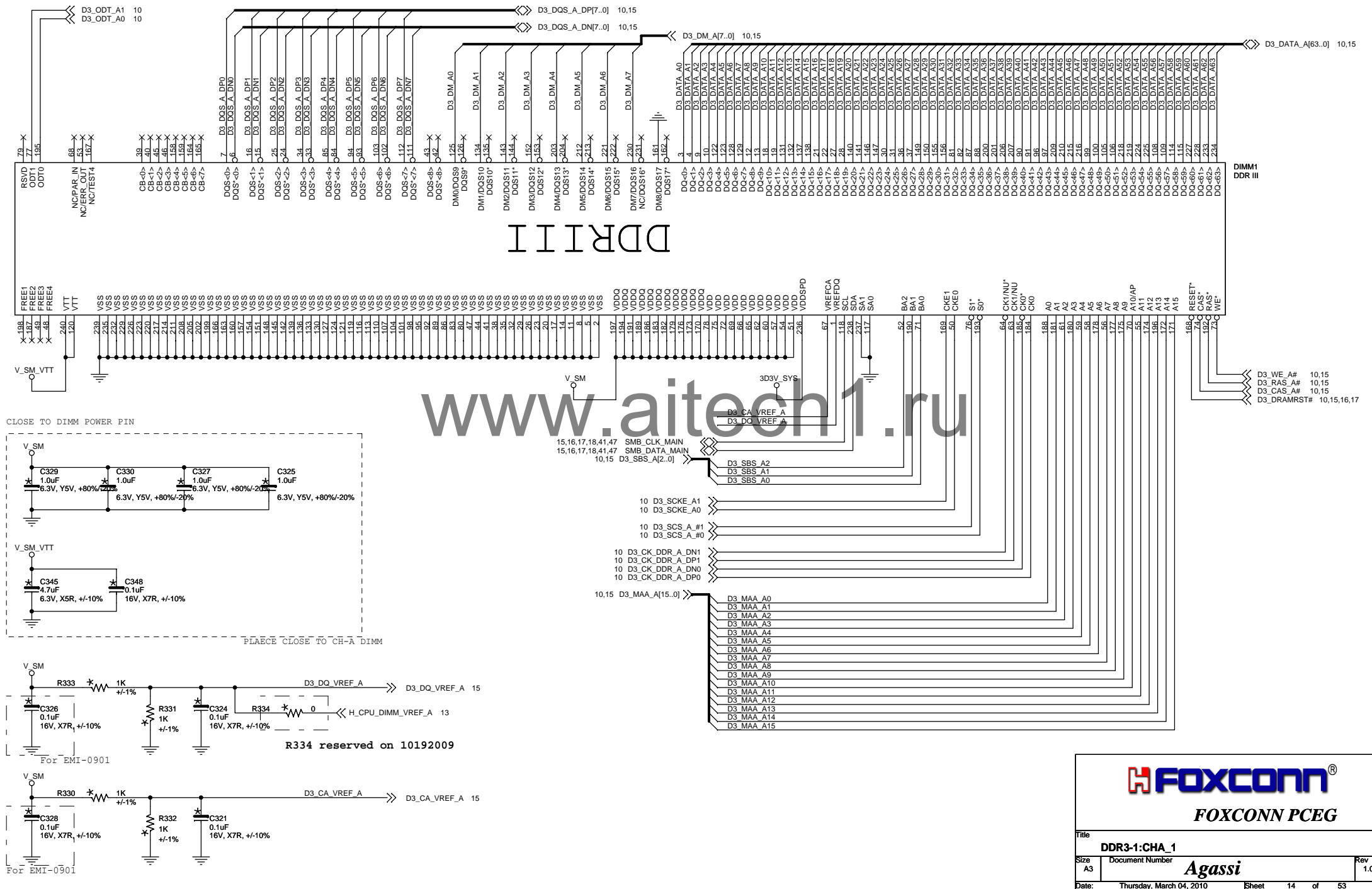
Title		CPU-5:POWER	
Size	A3	Document Number	Agassi
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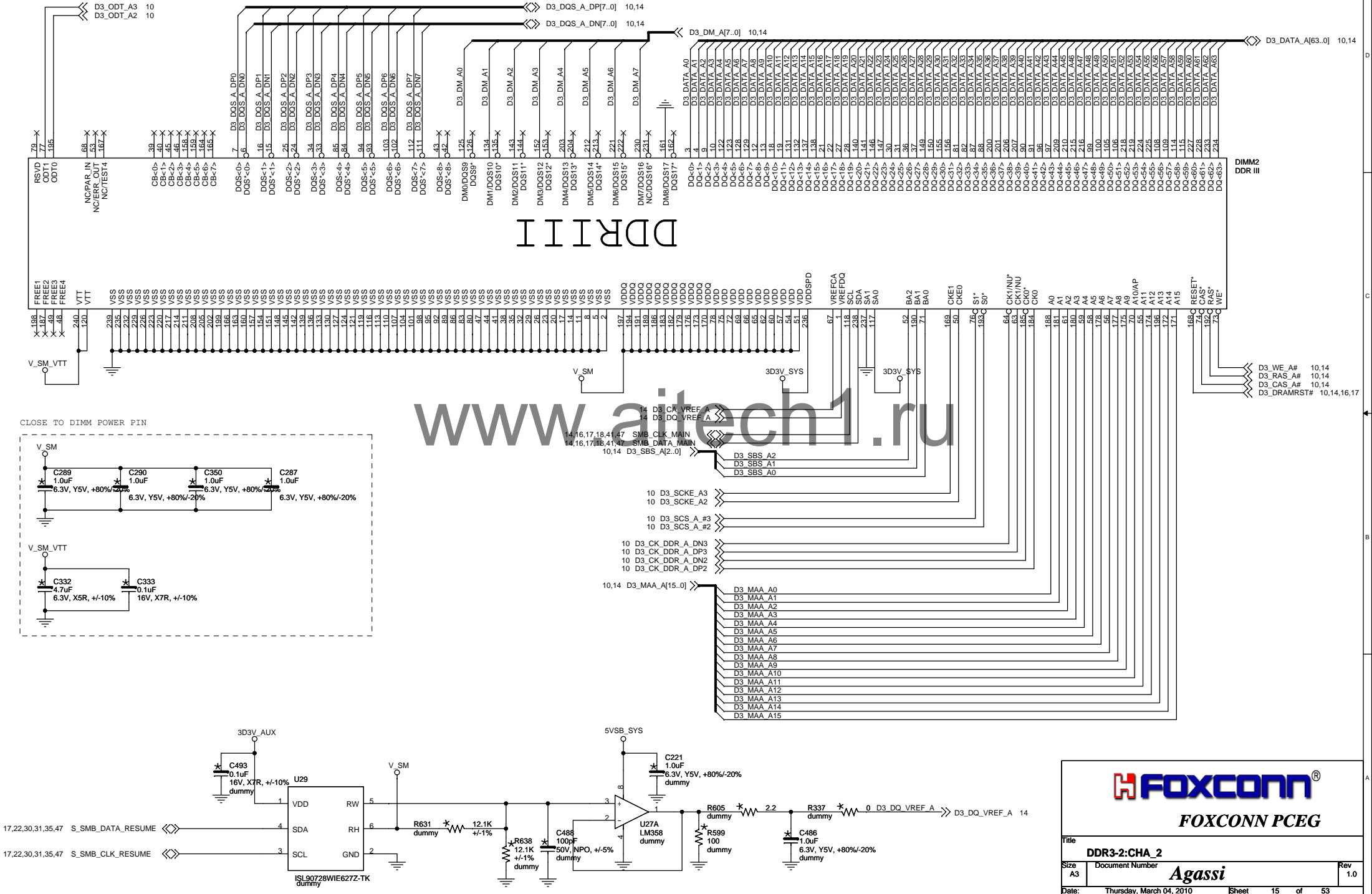



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Title		CPU-6:GND	
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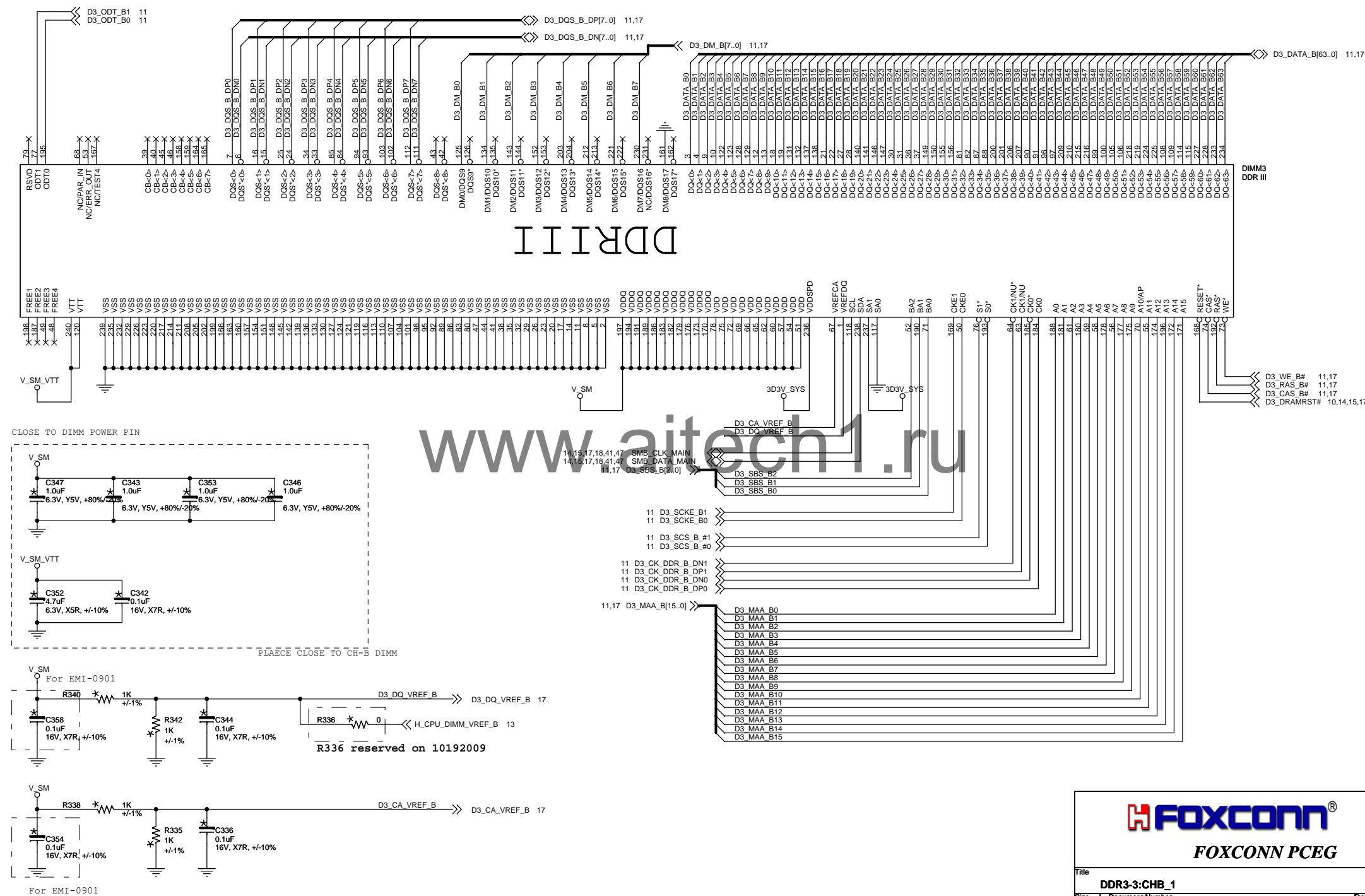
**FOXCONN PCEG**

Title: **DDR3-2:CHA\_2**

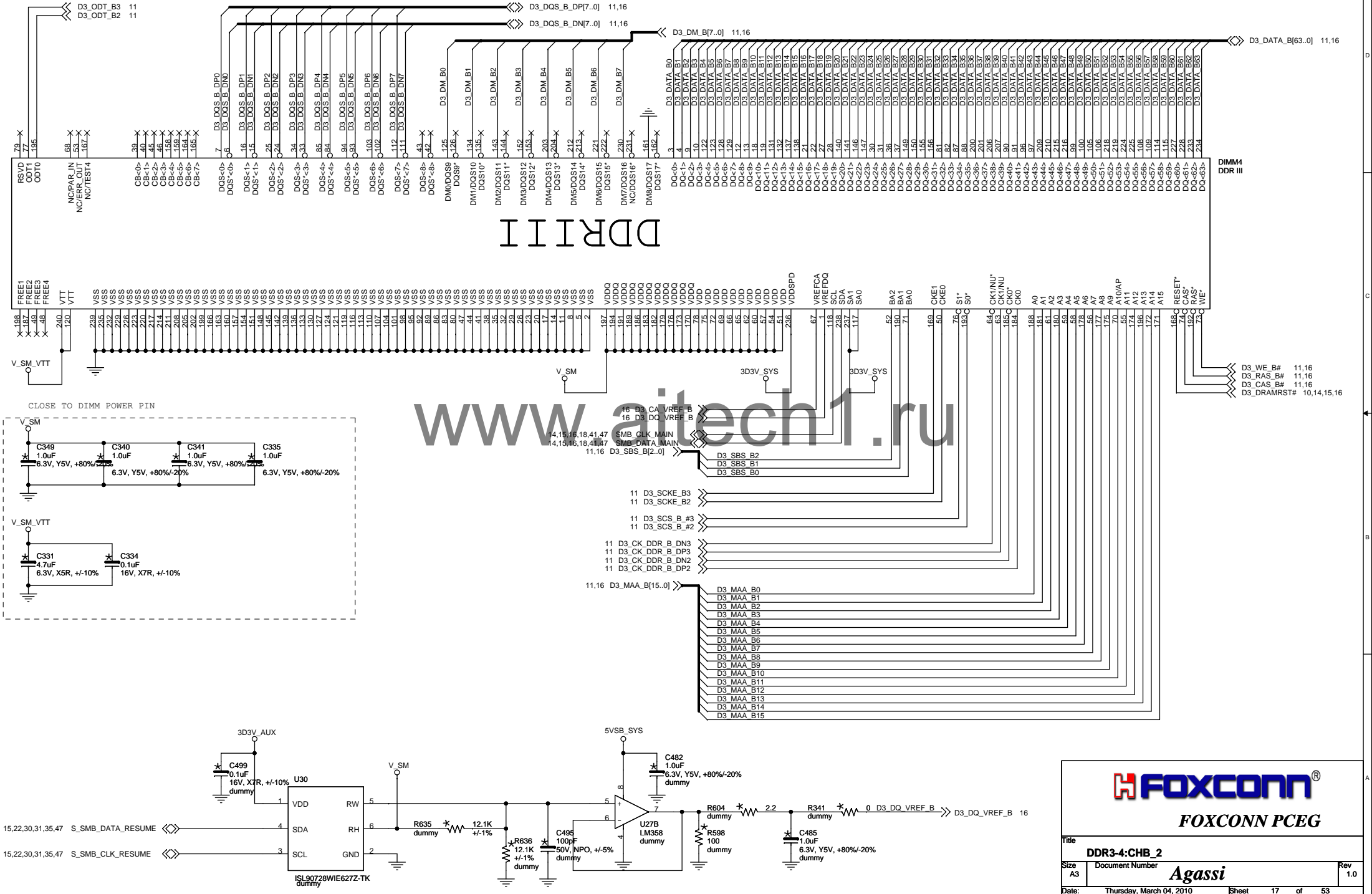
Size A3: Document Number **Agassi**


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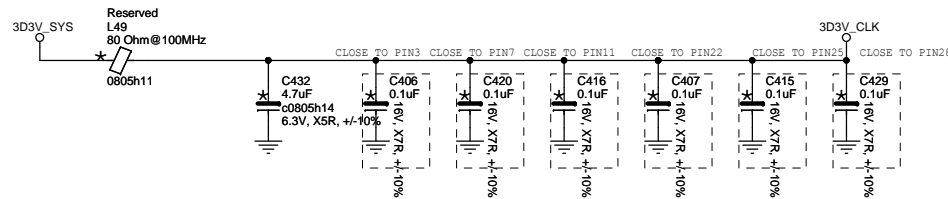


**FOXCONN PCEG**

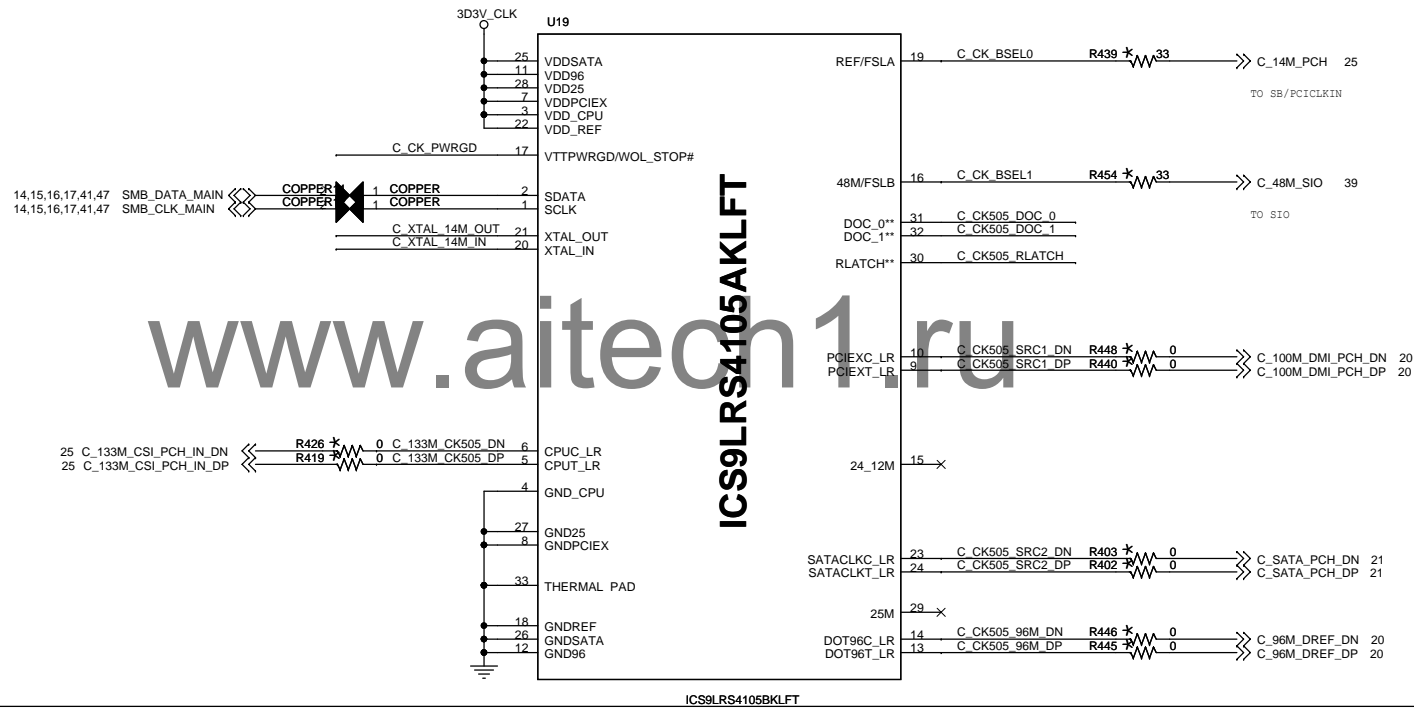
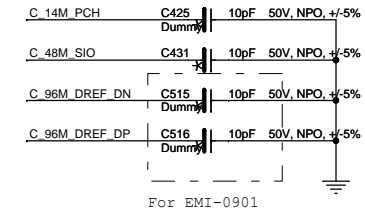
Title: **DDR3-4:CHB\_2**

Size A3: Document Number **Agassi**

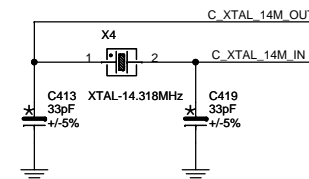
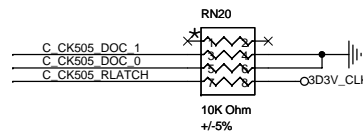
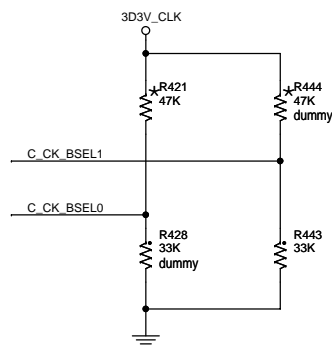
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for EMI



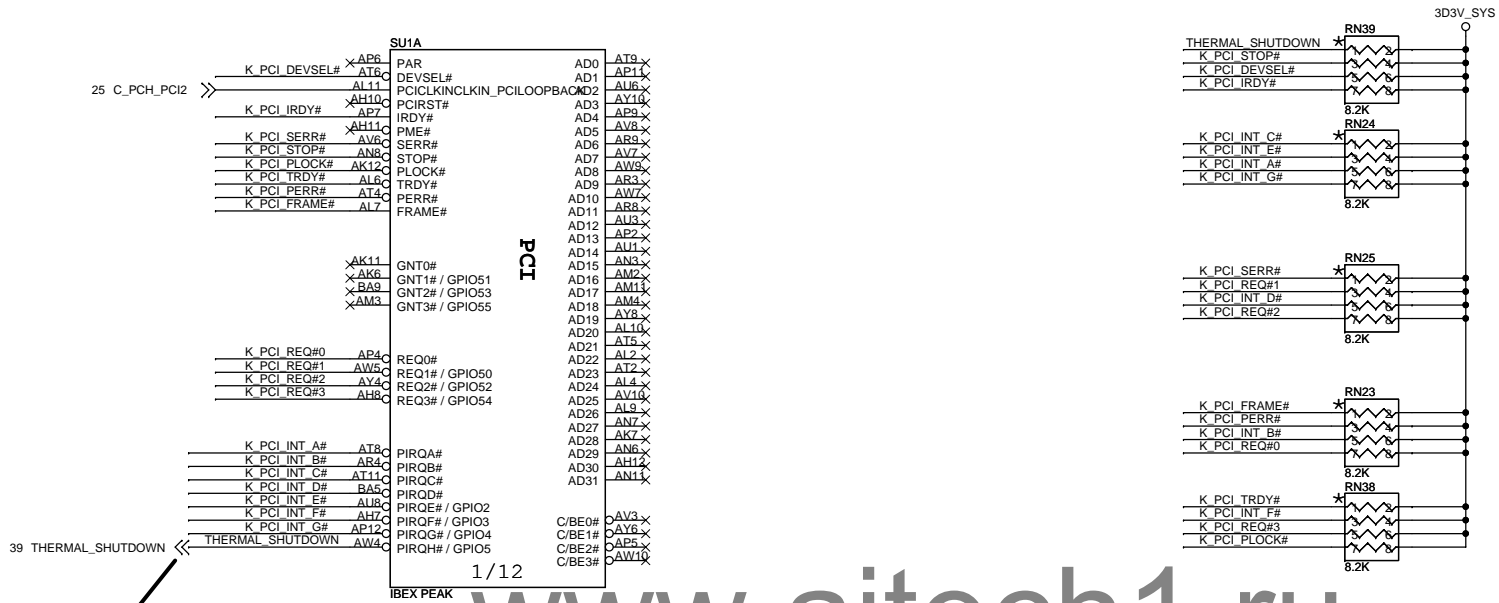
FREQ	BSEL0	BSEL1
100	1	1
133	1	0



$$C_e = 2 * 20 \text{ pF} - 7 \text{ pF} = 40 \text{ pF} - 7 \text{ pF} = 33 \text{ pF}$$

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FOXCONN PCEG

Title	CLOCK GEN
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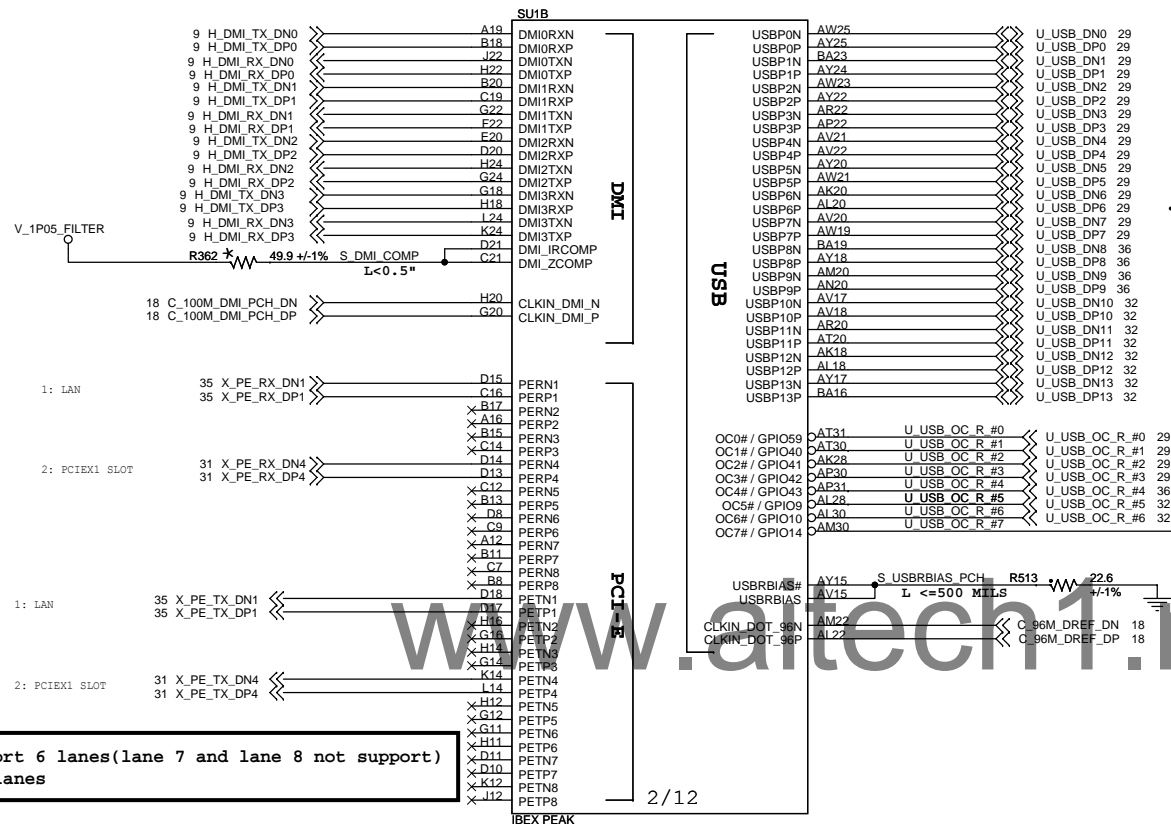


THERMAL\_SHUTDOWN need to be GPIO0~15 of IBEX PEAK

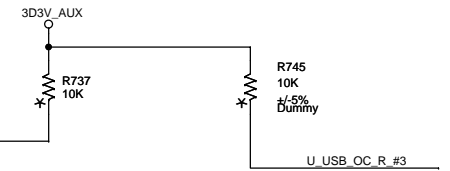


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Title		PCH-1:PCI	
Size	A3	Document Number	Agassi
Date:	Thursday, March 04, 2010	Sheet	19 of 53
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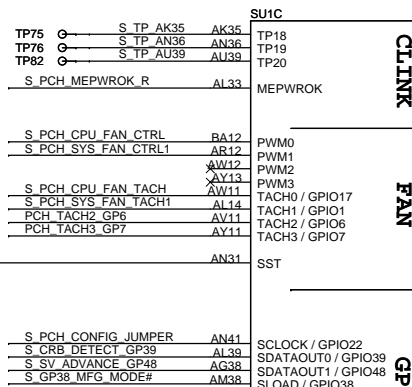
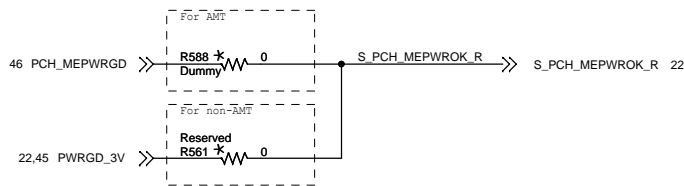


H55 chipset not support USB port6 and 7  
H57 support



H55 only support 6 lanes(lane 7 and lane 8 not support)  
H57 support 8lanes





CLINK

FAN

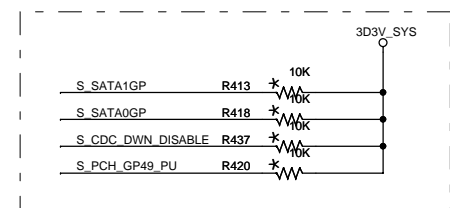
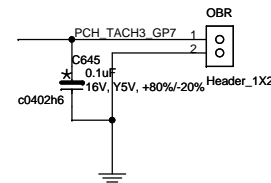
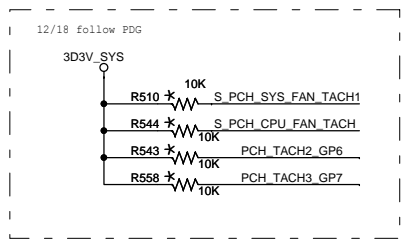
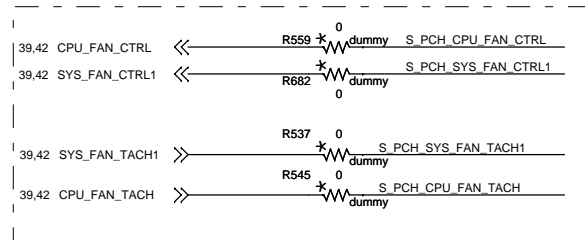
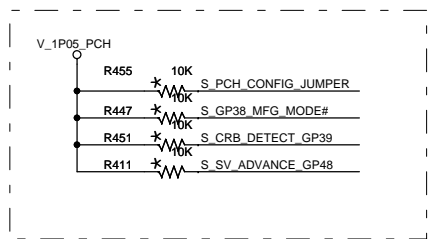
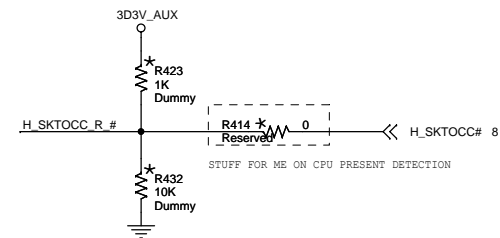
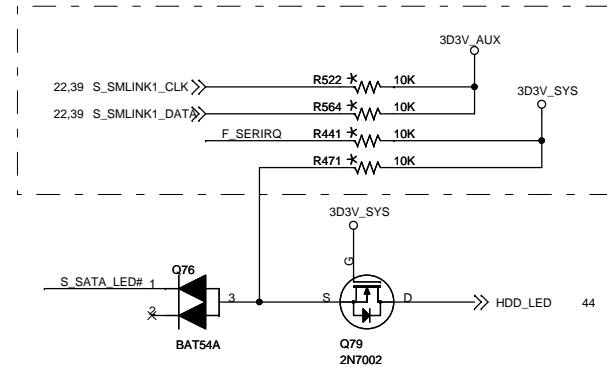
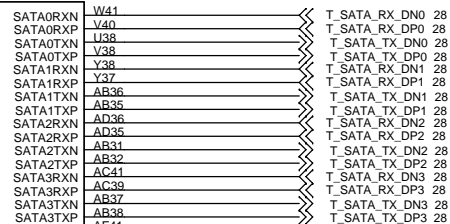
GPIO

SATA

HOST

3/12

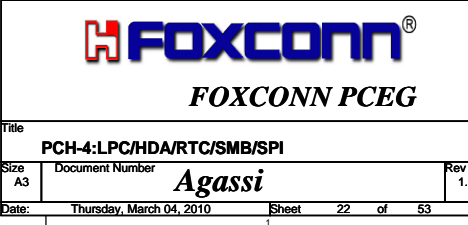
IBEX PEAK



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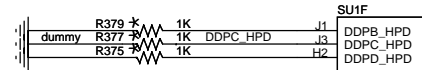
Title		PCH-3:SATA/HOST/FAN	
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33 DDPC\_HPD

DDPC\_HPD



SU1F

DDPB\_HPD

DDPC\_HPD

DDPD\_HPD

M1 DDPA\_AUXP  
 M2 DDPA\_AUXN  
 M3 DDPC\_AUXP  
 M4 DDPC\_AUXN  
 M5 DDPA\_AUXP  
 M6 DDPA\_AUXN  
 M7 DDPC\_AUXP  
 M8 DDPC\_AUXN

K10 DDPA\_0P  
 K11 DDPA\_0N  
 K12 DDPA\_1P  
 K13 DDPA\_1N  
 K14 DDPA\_2P  
 K15 DDPA\_2N  
 K16 DDPA\_3P  
 K17 DDPA\_3N

E3 DDPC\_0P  
 E4 DDPC\_0N  
 E5 DDPC\_1P  
 E6 DDPC\_1N  
 E7 DDPC\_2P  
 E8 DDPC\_2N  
 E9 DDPC\_3P  
 E10 DDPC\_3N

C5 DDPA\_0P  
 C6 DDPA\_0N  
 C7 DDPA\_1P  
 C8 DDPA\_1N  
 C9 DDPA\_2P  
 C10 DDPA\_2N  
 C11 DDPA\_3P  
 C12 DDPA\_3N

M3 SDVO\_INTP  
 M4 SDVO\_INTN  
 N2 SDVO\_STALLP  
 N3 SDVO\_STALLN  
 I6 SDVO\_TVCLKINP  
 I7 SDVO\_TVCLKINN

I6 SDVO\_TVCLKINP  
 I7 SDVO\_TVCLKINN

DISPLAY

6/12

IBEX PEAK

CRT\_HSYNC

CRT\_VSYNC

CRT\_RED

CRT\_GREEN

CRT\_BLUE

CRT\_IRTN

AB4

AG4

AG2

DAC\_IREF

AF2

L&lt;500 MILLS

NON-Graphic sku : Change to 0 ohm

P12

P13

T13

TP\_T12

TP\_P12

TP\_P13

TP\_T13

TP\_T12

TP\_P12

TP\_P13

TP\_T13

TP\_T12

TP\_P12

TP\_P13

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TP\_P13

TP\_T13

TP\_T12

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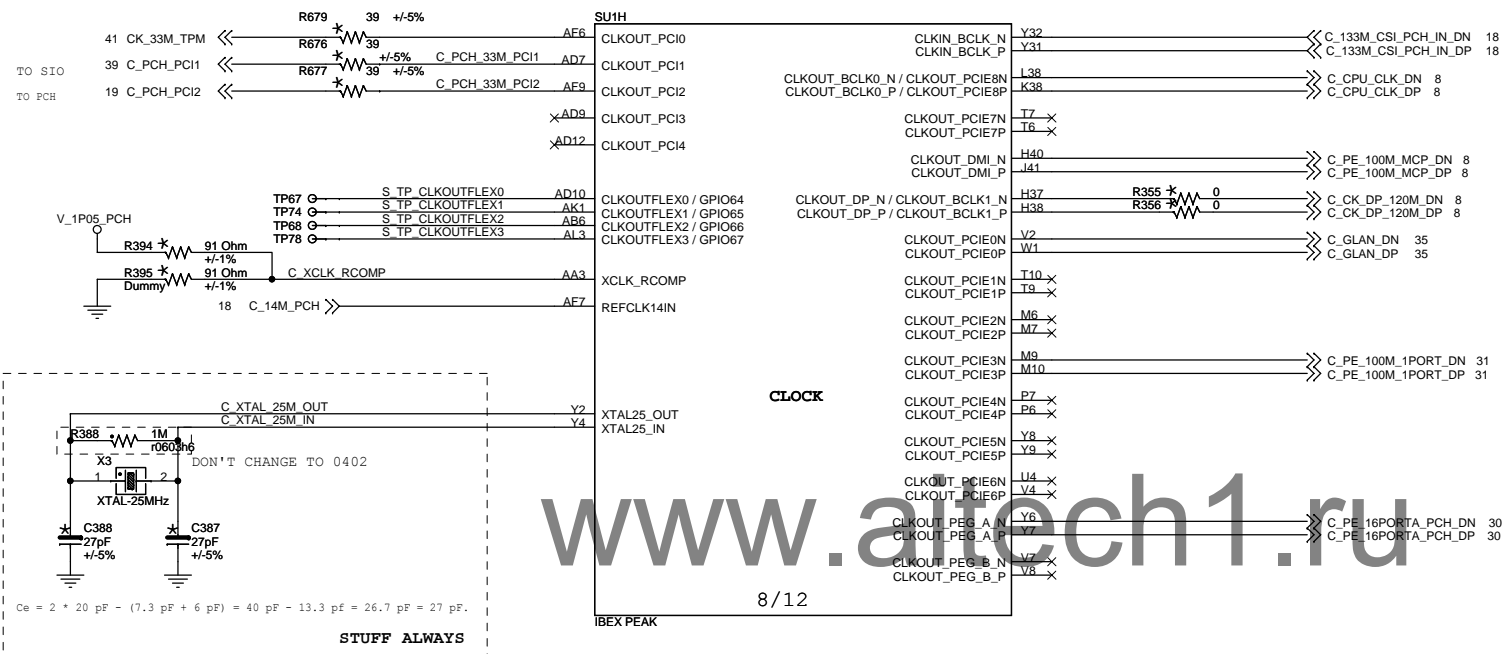
TP\_T13

TP\_T12

TP\_P12

TP\_P13





**FOXCONN**

**FOXCONN PCEG**

Title  
**PCH-7:CLOCK**

Size A3 Document Number

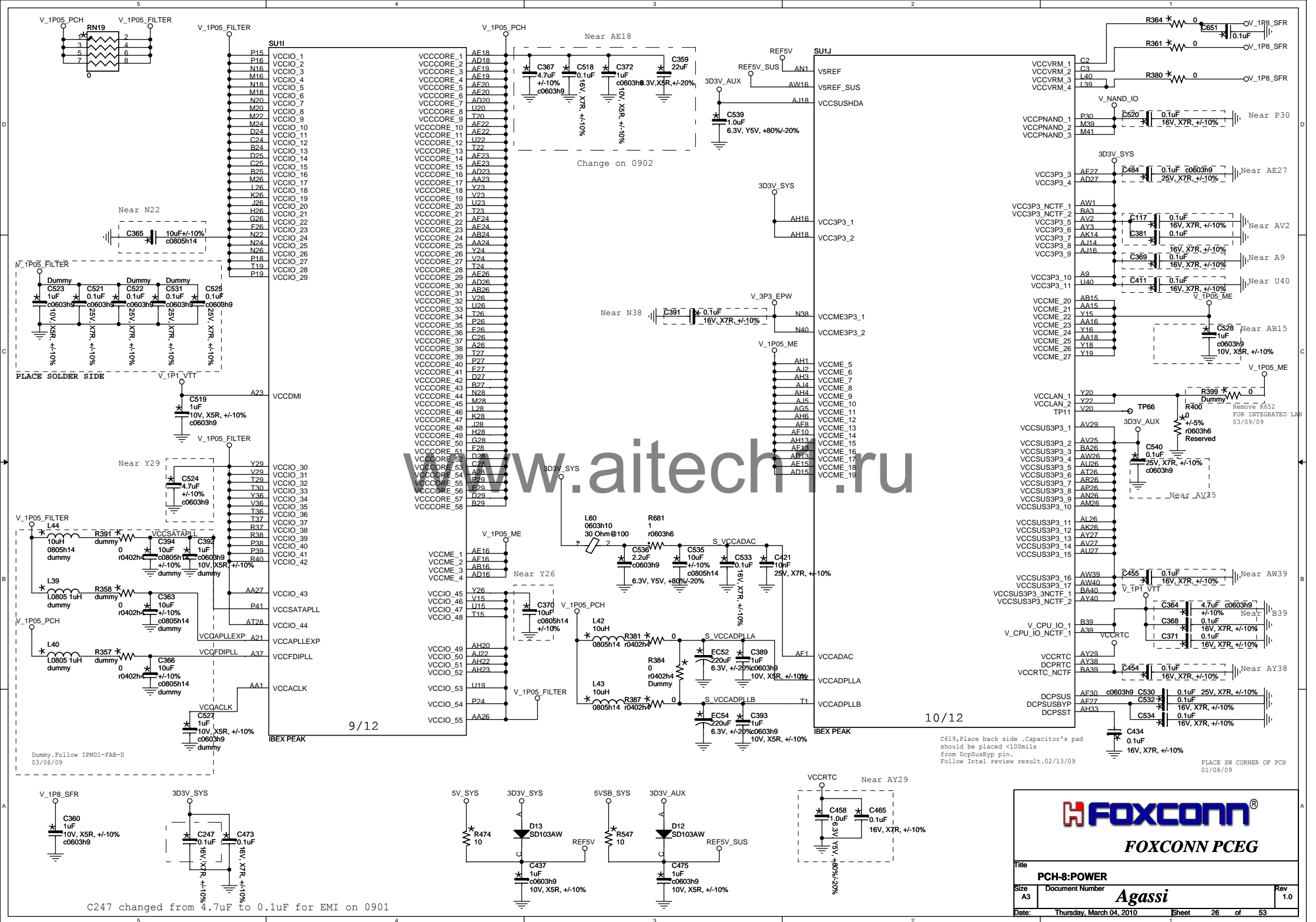
**Agassi**

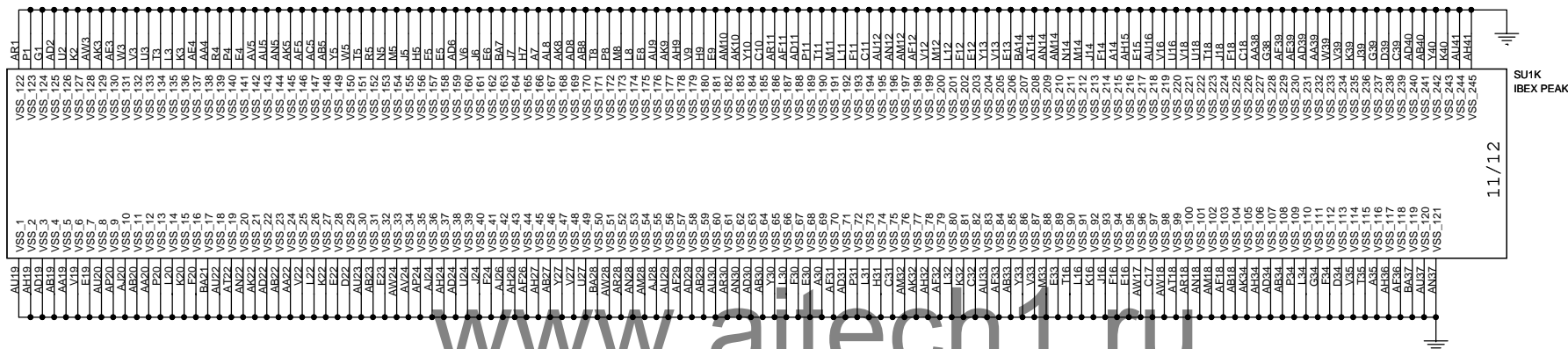
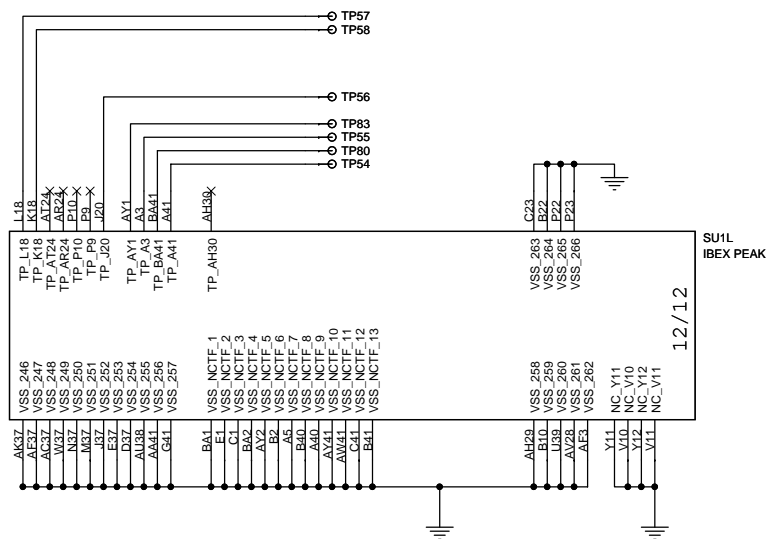
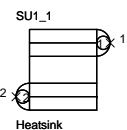
Rev

1.0

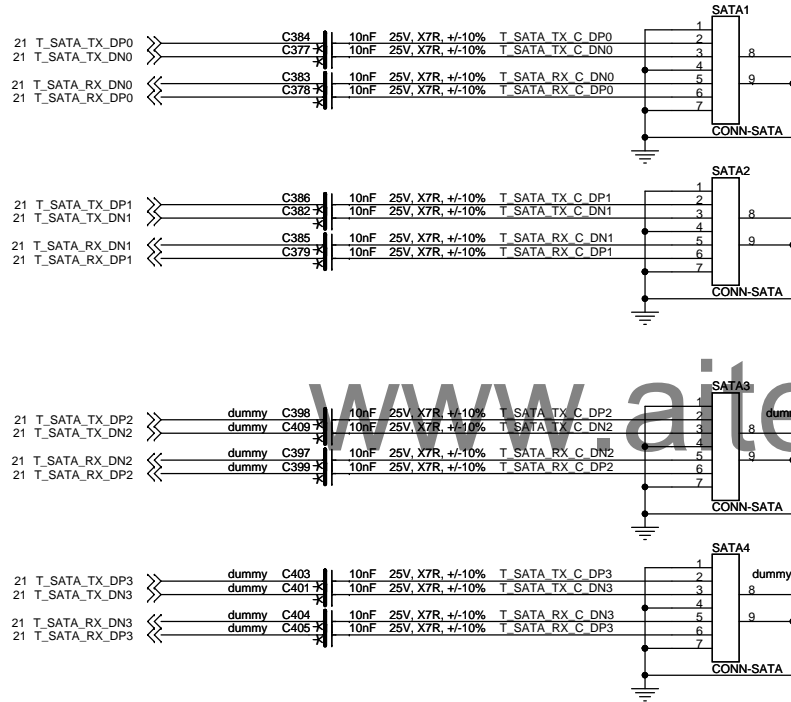
Date: Thursday, March 04, 2010

Sheet 25 of 53





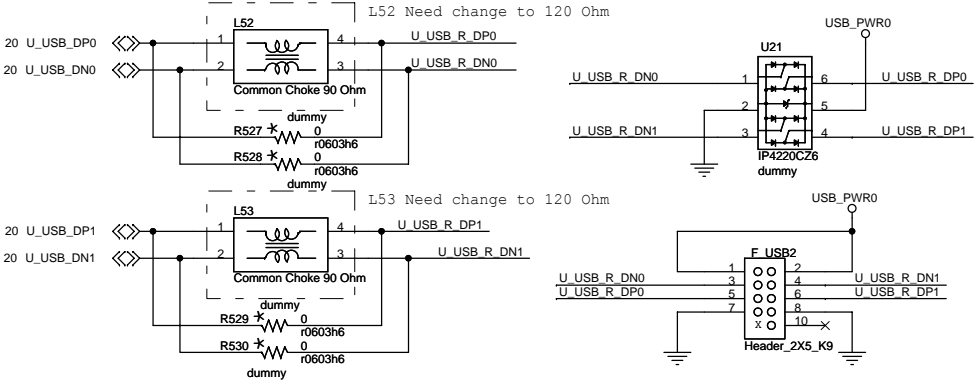
BLUE



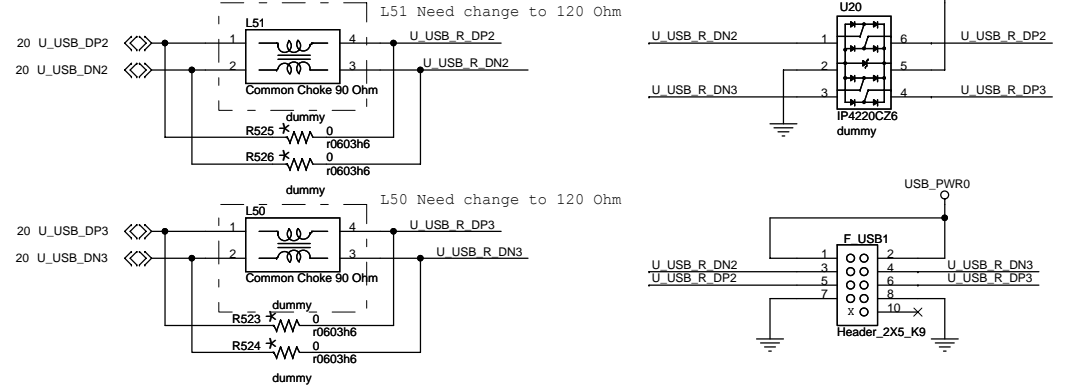
FOXCONN PCEG

Title			SATA CONNECTOR
Size	Document Number	Agassi	
A3			Rev 1.0
Date:	Thursday, March 04, 2010	Sheet 28 of 53	

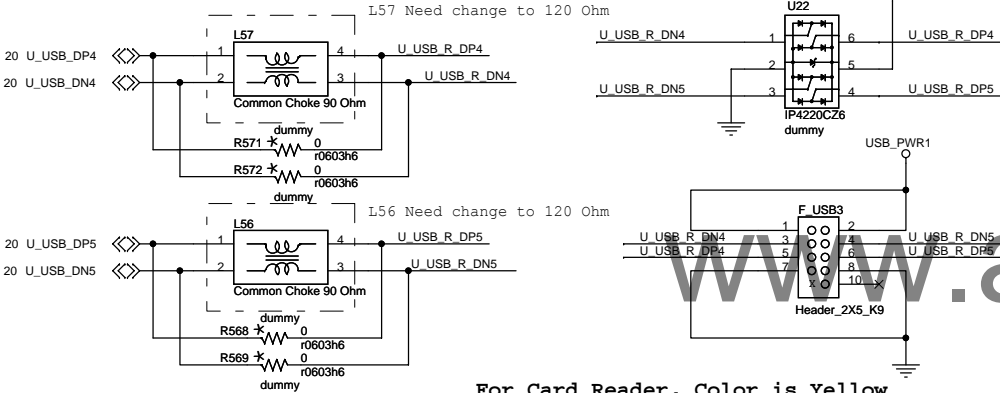
FRONT USB HEADER #2



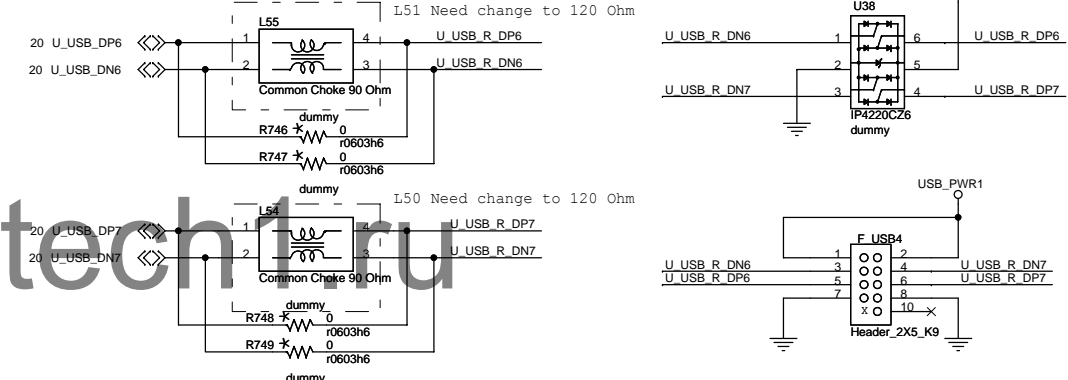
FRONT USB HEADER #1



FRONT USB HEADER #3

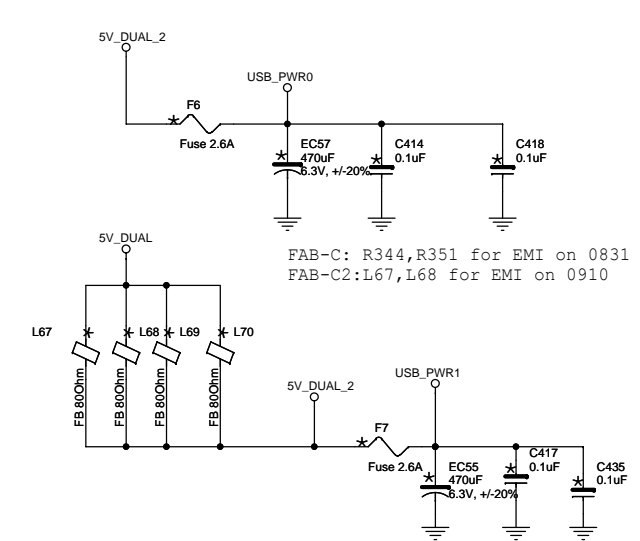


FRONT USB HEADER #4

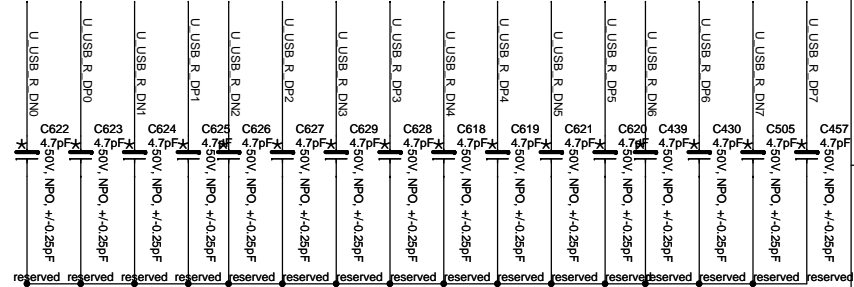
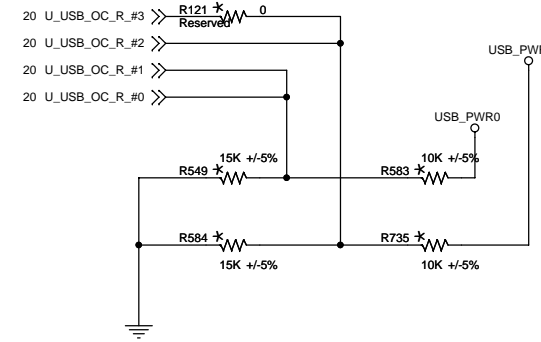


For Card Reader, Color is Yellow

FRONT USB POWER



F-USB OC

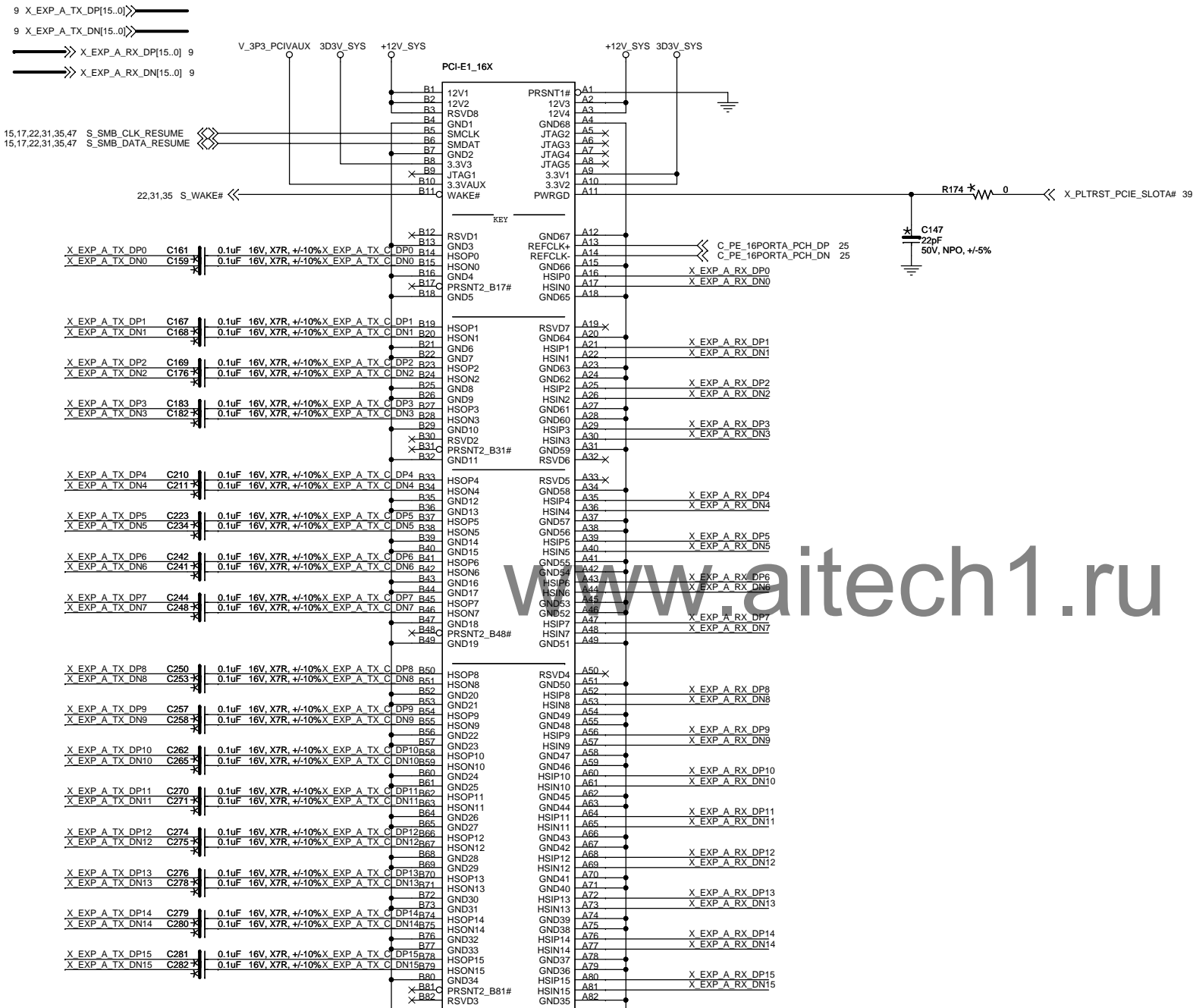


**FOXCONN PCEG**

Title: **USB:FRONT USB HEADER 1/2/3/4**

Size A3 Document Number: **Agassi** Rev 1.0

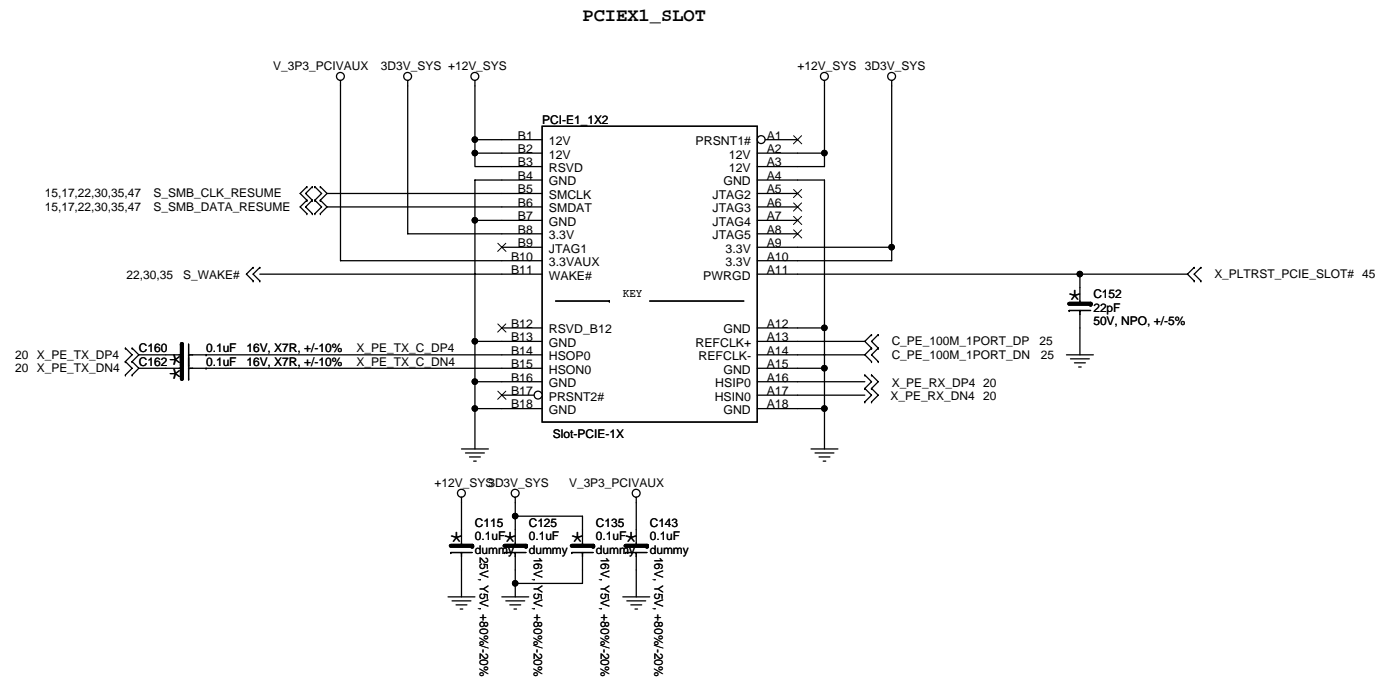
Date: Thursday, March 04, 2010 Sheet 29 of 53



**FOXCONN**

**FOXCONN PCEG**

Title		PCIE X16 SLOT
Size	Document Number	Agassi
A3		Rev 1.0
Date:	Thursday, March 04, 2010	Sheet 30 of 53

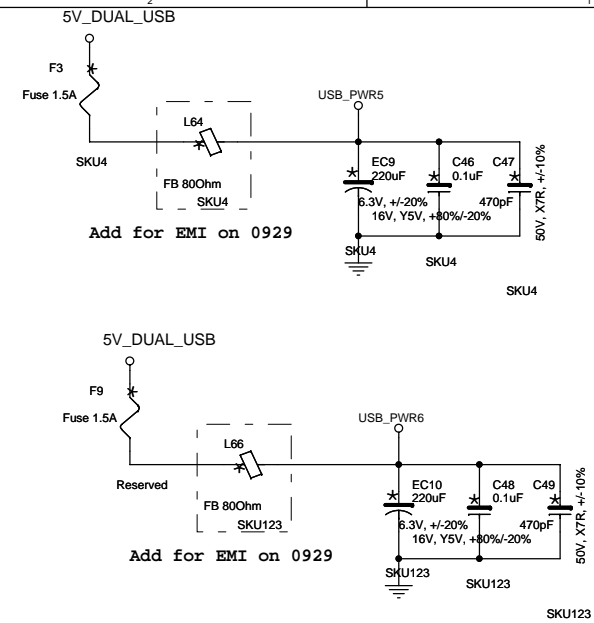
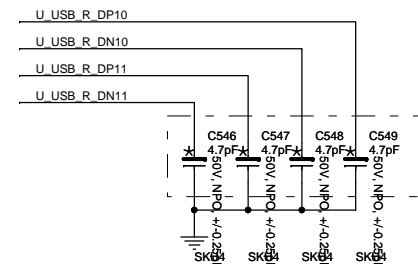
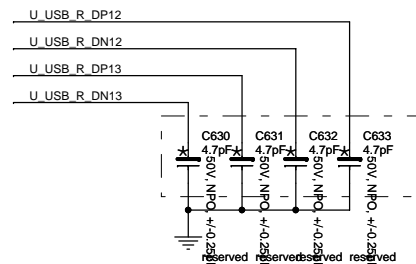
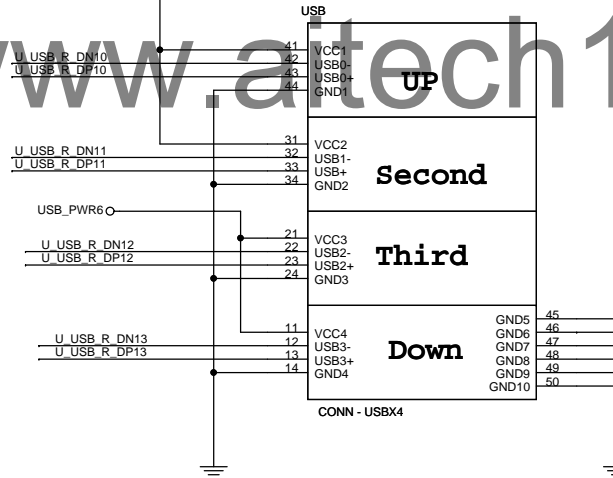
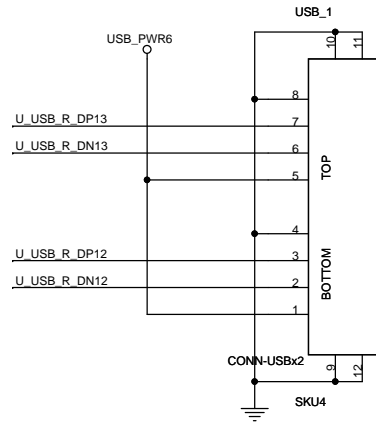
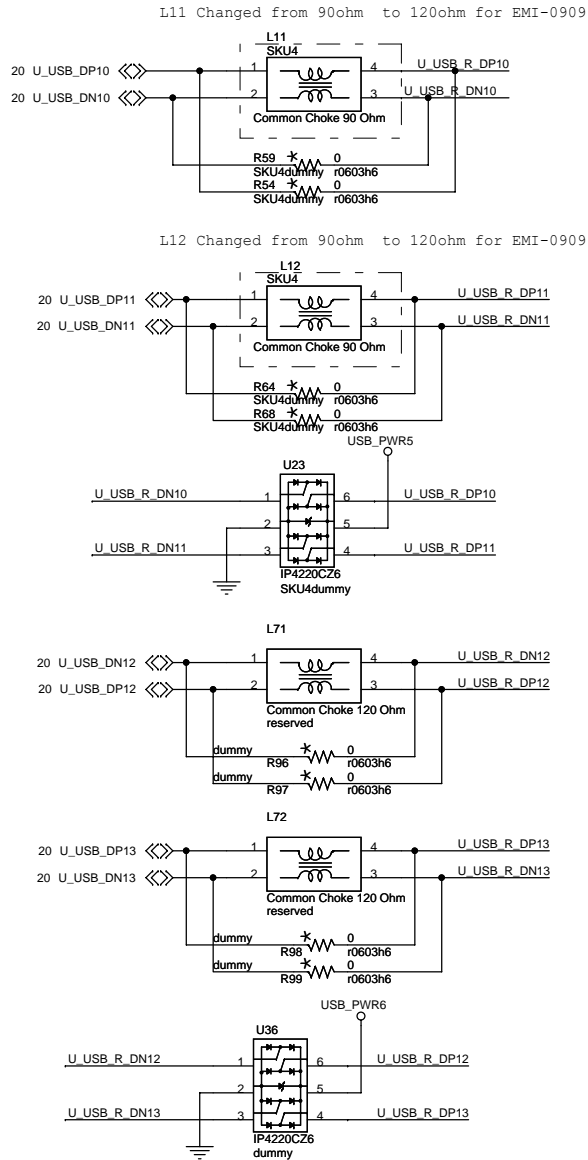


**FOXCONN PCEG**

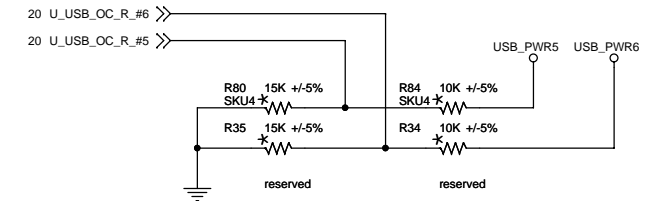
Title		PCIE X1 SLOT 1/2	
Size	A3	Document Number	Agassi
Date:	Thursday, March 04, 2010	Sheet	31 of 53
Rev	1.0		

## Rear USB connector X2

Change U18 and U17 from 90 to 120ohm for EMI-060926



## Rear USB OC



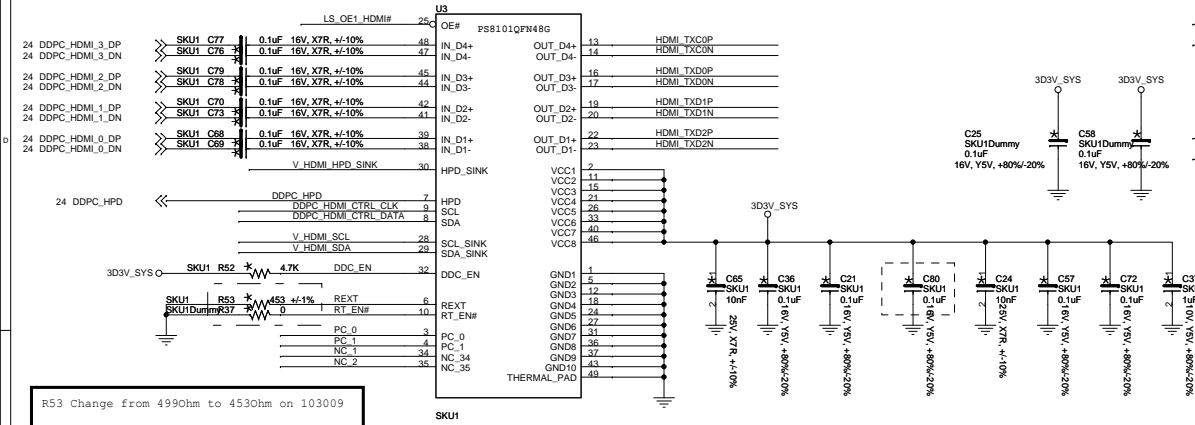
**FOXCONN**

**FOXCONN PCEG**

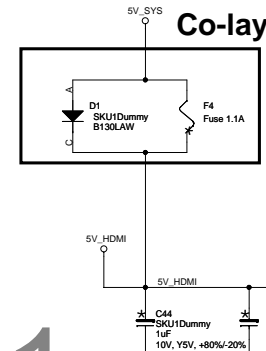
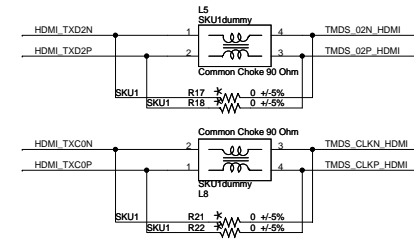
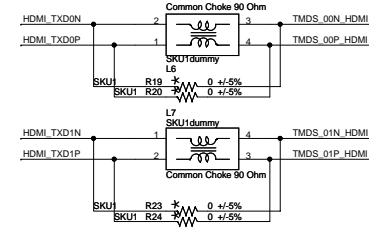
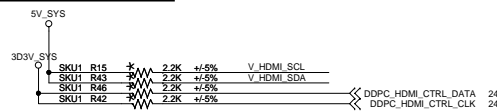
Title		eSATA_USB CONN	
Size	A3	Document Number	Agassi
Date:	Thursday, March 04, 2010	Sheet	32 of 53
Rev	1.0		



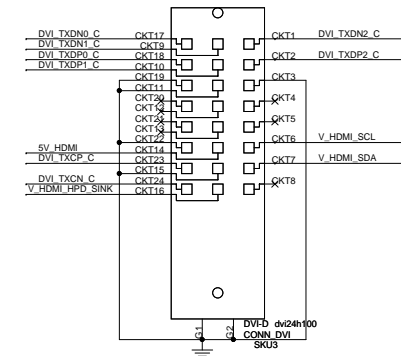
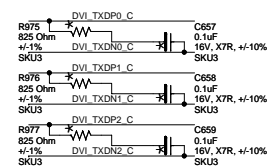
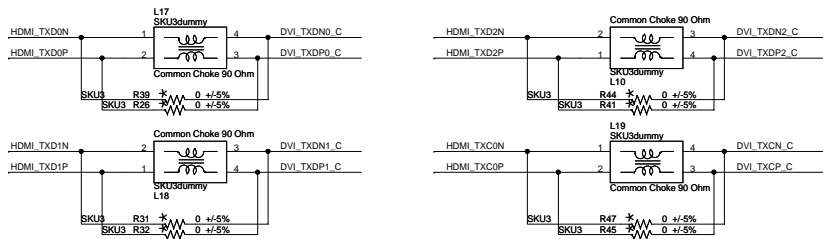
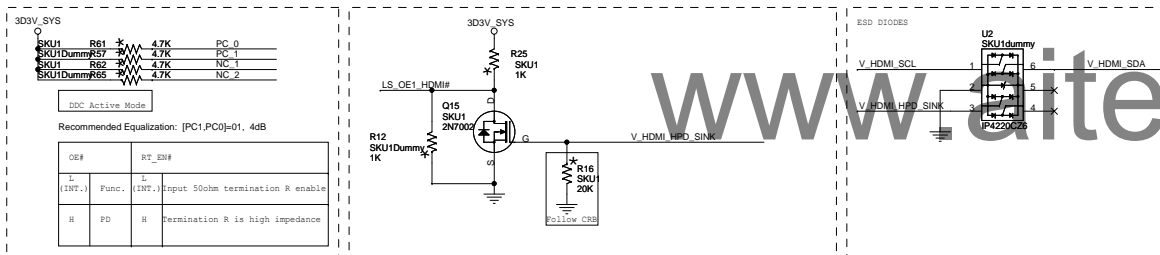
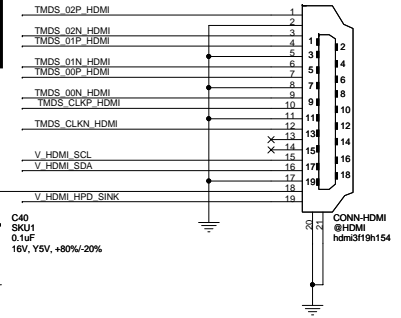
## HDMI Level shift



R53 Change from 4990hm to 4530hm on 103009



## HDMI Connector



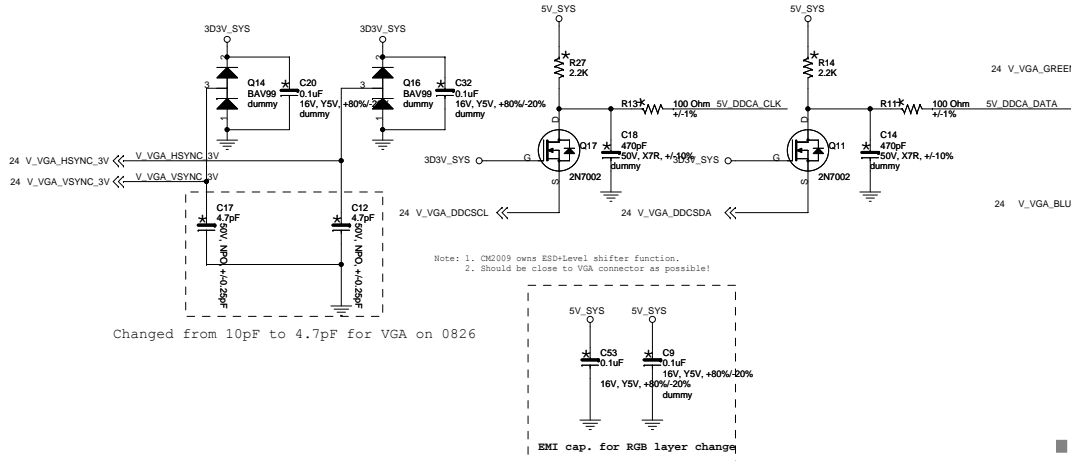
**FOXCONN PCEG**

Title			
HDMI connector			
Size C	Document Number		Rev
	Agassi		1.0
Date:	Thursday, March 04, 2010	Shot	3% of 4%

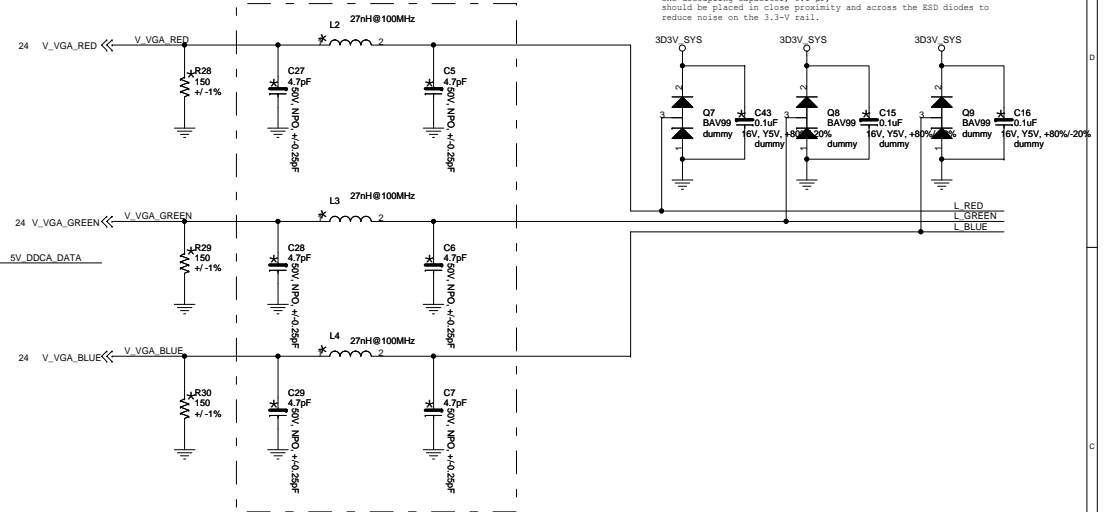
# RGB routing

1. Match the trace lengths within CRT\_RED, CRT\_GREEN and CRT\_BLUE to 200 mils (0.508 cm).
2. Match the trace lengths of CRT SYNC signals with CRT DAC signals to 200 mils (0.508 cm).
3. All length matching is based on Ibex Peak die-pad to CRT connector routing length and thus includes package length compensation.

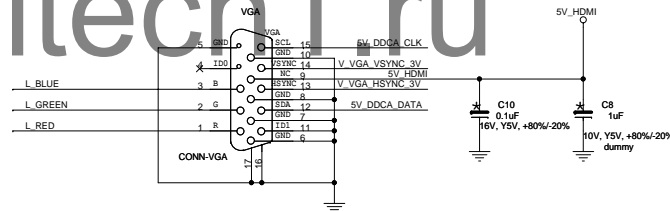
ESD diodes are required for each CRT DAC output. The diodes should connect between the 3.3-V power plane (from the regulator) and ground. These diodes should have a low C rating ( $\leq 5$  pF max) and a small leakage current ( $\sim 10$   $\mu$ A at 120°C). The diodes should be placed to keep the inductance of the 3.3-V power rail connection as low as possible. These diodes should be placed between the analog switch and the VGA connector, preferably near the respective VGA connector. In addition, one decoupling capacitor,  $C1 = 0.1$   $\mu$ F, should be placed in close proximity and across the ESD diodes to reduce noise on the 3.3-V rail.



Changed for VGA on 0826



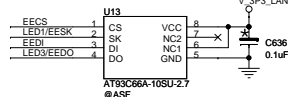
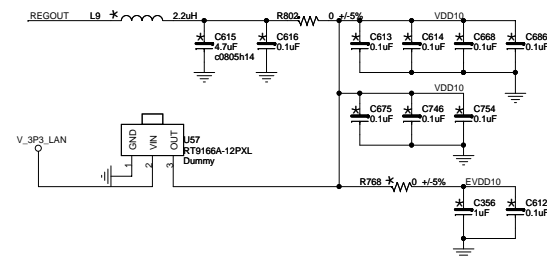
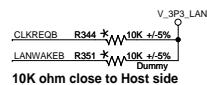
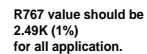
## VGA Connector



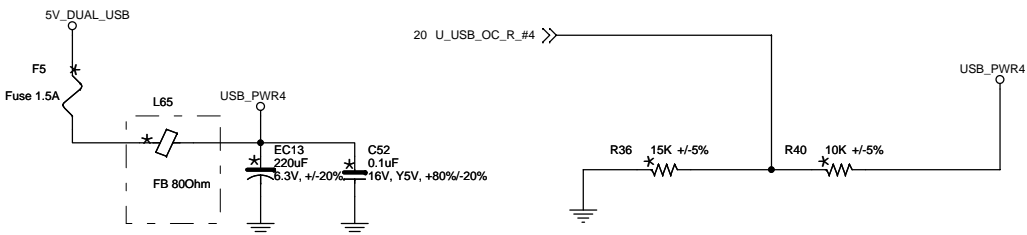
**FOXCONN**

FOXCONN PCEG

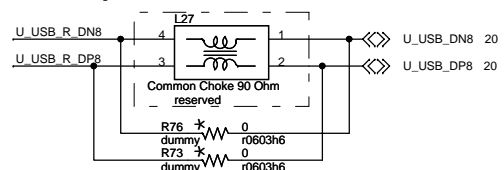
File	VGA connector		
Size	Document Number	Agassi	Rev 1.0
Date	Thursday, March 04, 2010	Sheet 34 of 53	



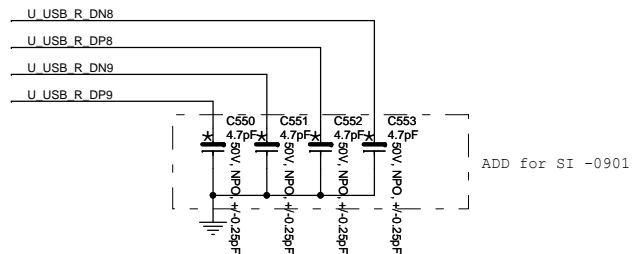
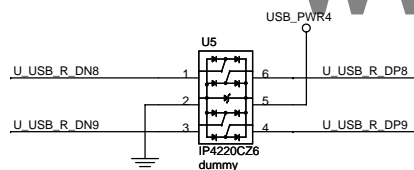
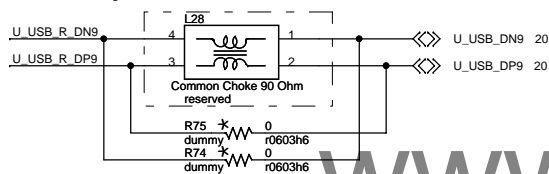
**LAN + 2USB CONNECTOR**



L27 changed from 90ohm to 120ohm for EMI-0909

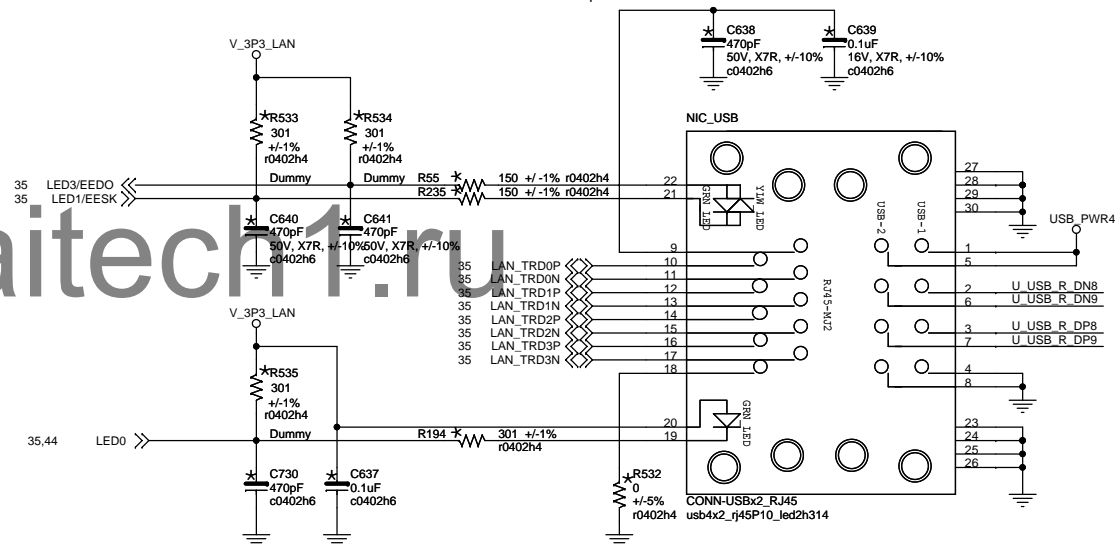


L28 changed from 90ohm to 120ohm for EMI-0909



## LAN CONN

OFF = LINK 10 Mbps  
GREEN = LINK 100 Mbps  
YELLOW = LINK 1000 Mbps



ACTIVE LED  
GREEN = LINK UP  
BLINKING = TX/RX ACTIVITY

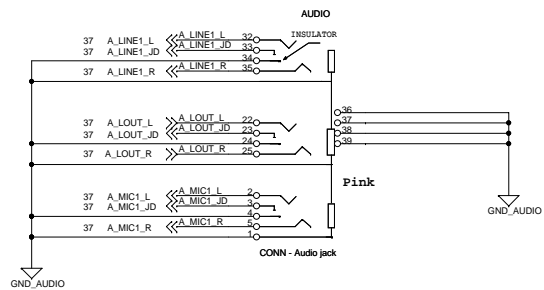


**FOXCONN PCEG**

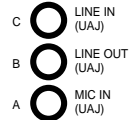
Title			
LAN-2:CONNECTOR WITH USB			
Size A3	Document Number	Agassi	Rev 1.0
Date:	Thursday, March 04, 2010	Sheet	36 of 53



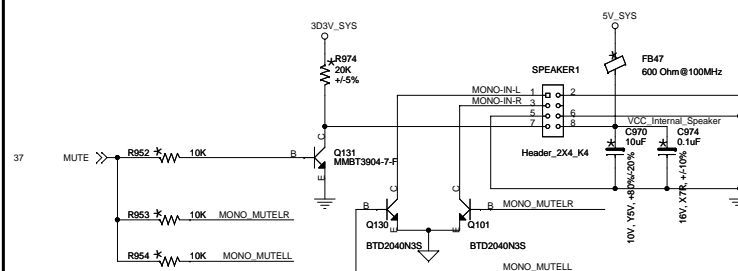
## Audio CONN (3 Port)



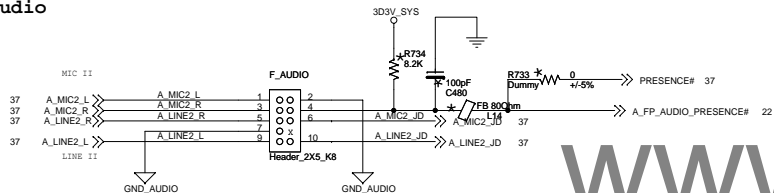
### Audio Jack



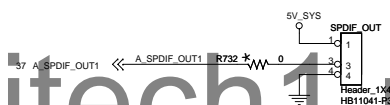
37 A\_SURR\_LC << A\_SURR\_LC C33.1 2 1uF c0603h9 MONO-IN-L  
37 A\_SURR\_RC << A\_SURR\_RC C61.1 2 1uF c0603h9 MONO-IN-R



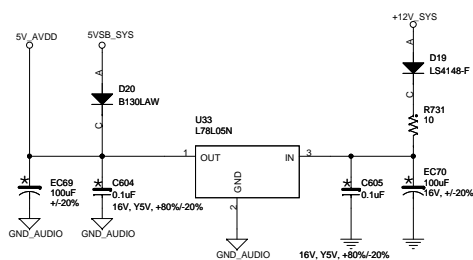
## Front\_Audio



## SPDIF\_OUT



## 12V to 5V Power Regulator



**FOXCONN**

FOXCONN PCEG

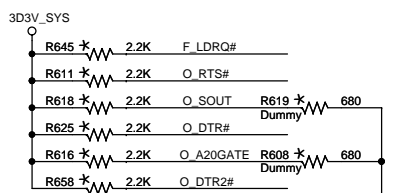
File	Document Number	Rev
Size	Document Number	Rev
C	Agassi	1.0
Date:	Thursday, March 04, 2010	Sheet 38 of 53

## IT8720 Power On Strapping Options

Symbol		value	Description
JP1 (pin 38)	Flashseg1_EN	1	Disable
		0	Flash I/F Address Segment1 is enable
JP3 Pin 124	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 is enabled
JP4 Pin 126	K8PWR_EN	1	K8 power sequence function is disabled
		0	K8 power sequence function is enabled
JP3 & JP5 Pin 124 & 46	FAN_CTL_SEL	11	The default value of EC Index 15h/16h/17h is 40h
		10	The default value of EC Index 15h/16h/17h is 7Fh(Fan off )
		01	The default value of EC Index 15h/16h/17h is 00h(Fan full speed )
		00	The default value of EC Index 15h/16h/17h is 20h
JP5 Pin46	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK
JP2/JP6 Pin122/Pin29	SVID_EN	11	Disable VID/SVID out pins
		01	For Intel Platform Enable VIDEO0-VID07 output pins.
		10	For AMD Platform(always serial output) Enable SVD(Pin3)/SVC(Pin31)Output pins
		00	For AMD Platform(Serial-IN/Serial-Out and Parallel-IN/Parallel-Out It is selected by CPU

```
Follow ITE:
R683 changed from 2.2K to 4.7K
Pull changed from 3D3V_SYS to 3D3V_AUX on 0929
```

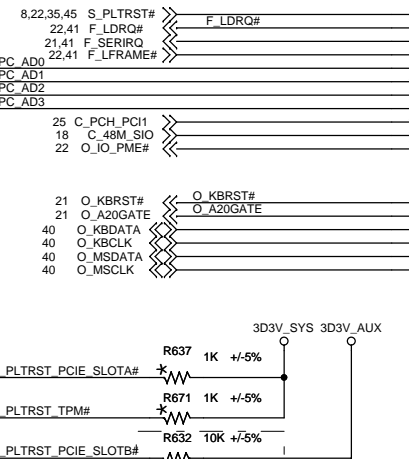
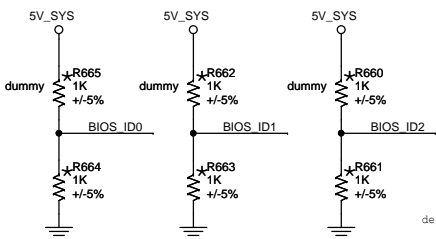
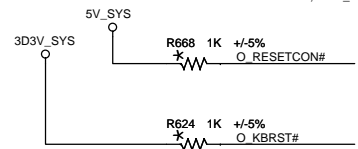
Follow ITE:  
R633 changed from 10K to 4.7K  
Pull changed from 5V\_SYS to 3D3V\_SYS on 0929



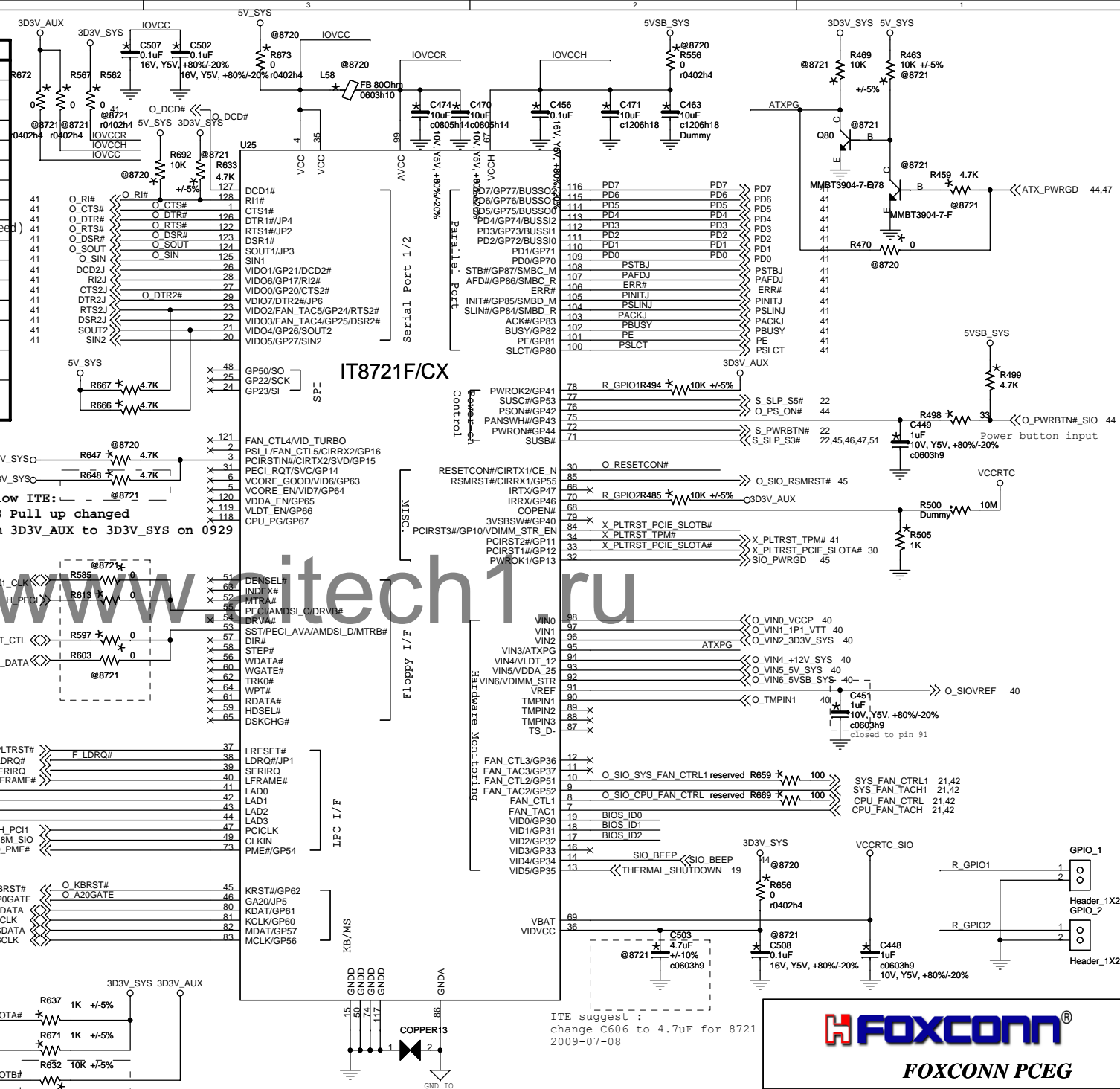
```

| If without use these pins, Please pull-up to VCC.
| Don't let it floating
| 1.Pin 30:RESETCON#
| 2.Pin 95:VIN3/ATXPG
| 3.Pin 71:SUSB#
| 4..Power On Strapping Options pin

```



R632 changed from 1K to 10K for EUP on 0929



ITE suggest :  
change C606 to 4.7uF for 8721  
2009-07-08



**FOXCONN PCEG**

Title	<b>SIO-1:ITE8720</b>
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Size	Document Number
10	

## Agassi

Rev	1.0
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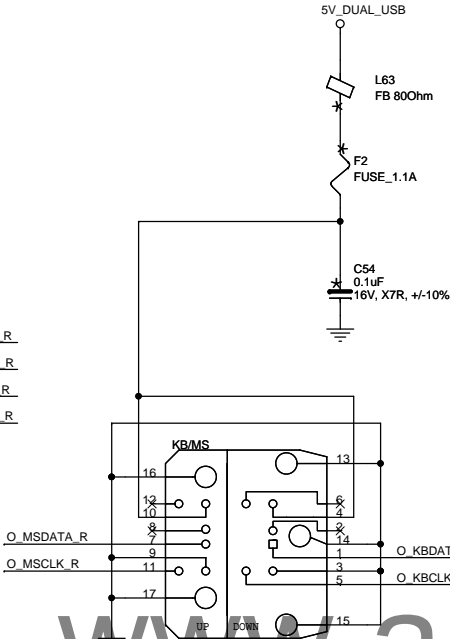
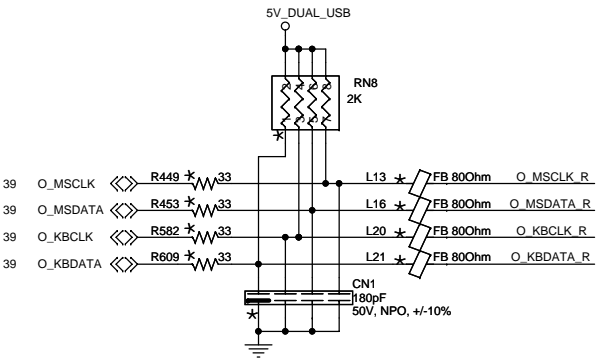
Date: Thursday, March 04, 2010

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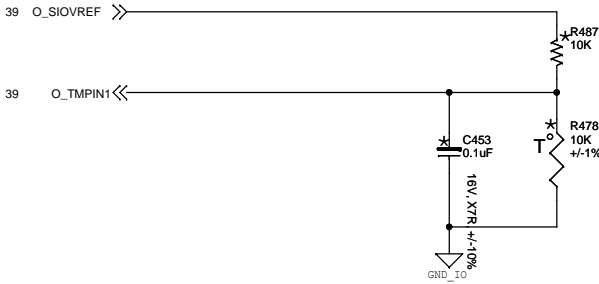

ITE8720 Colay ITE8721

L13,L14,L15.L16 change from 80ohm to 120ohm on 11052003

Add for EMI on 0929

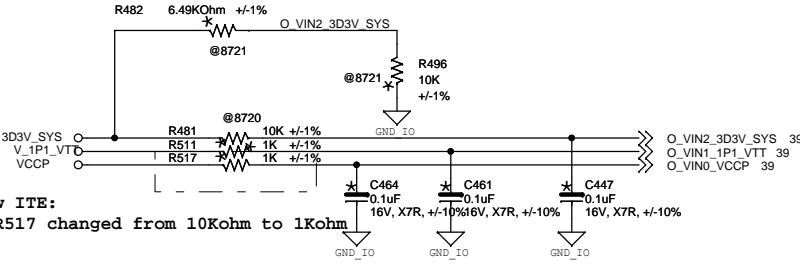


Temperature Monitor: Detect system temperature

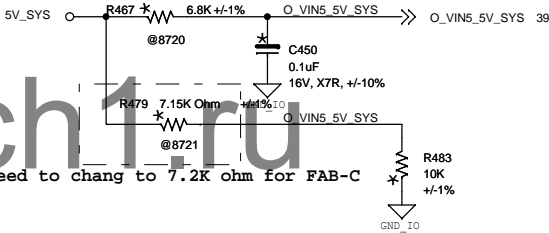
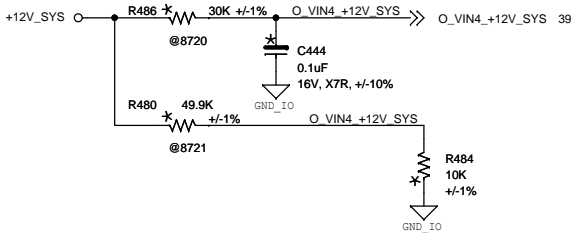


Voltage Monitor Detect:Vcore/+12V/+5V\_SYS/+3.3V\_SYS/1P1\_VTT/5VSB

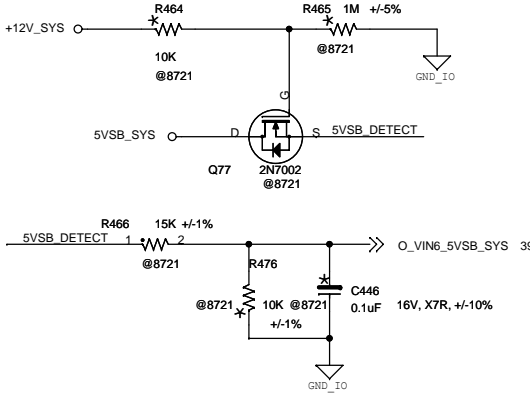
All parts close to SIO



Follow ITE:  
R511,R517 changed from 10Kohm to 1Kohm



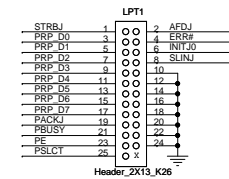
R479 need to chang to 7.2K ohm for FAB-C



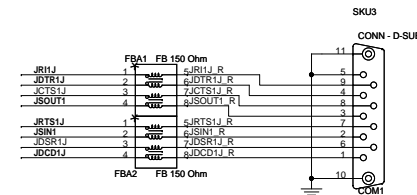
FOXCONN PCEG

Title		SIO-2:PS2/HW Monitor	
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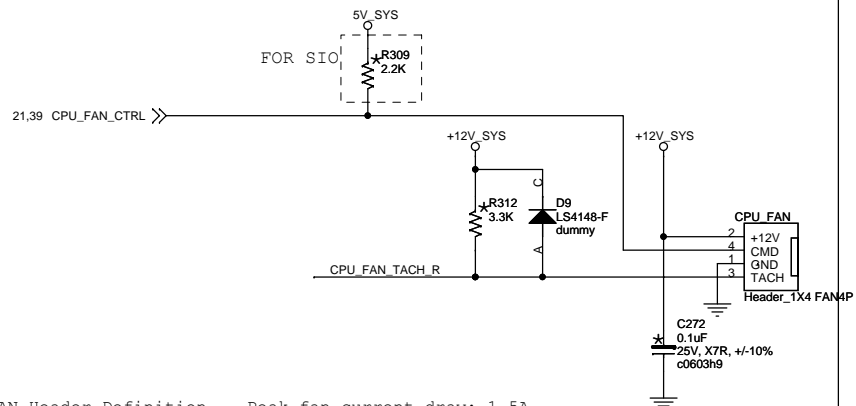


## Serial Port



## Serial Port

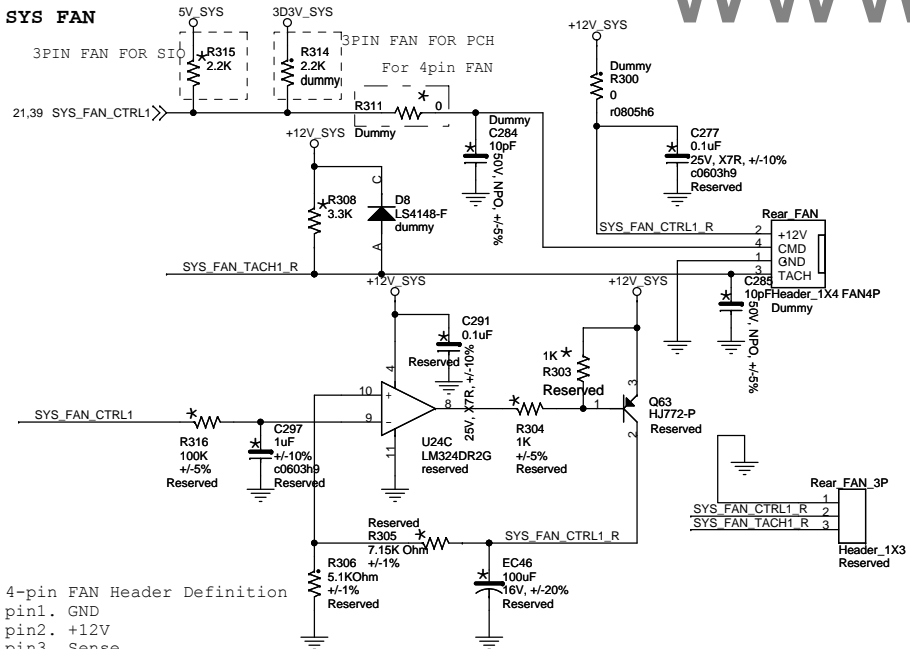
## CPU FAN



#### 4-pin FAN Header Definition

pin	Fan header Definition	Fan fan current draw: 1.1A
pin1.	GND	Average fan current draw: 1.1A
pin2.	+12V	Fan start-up current draw: 2.2A
pin3.	Sense	Fan start-up current draw maximum duration: 1.0 second
pin4.	Control	Fan header voltage: 12V +/- 10%

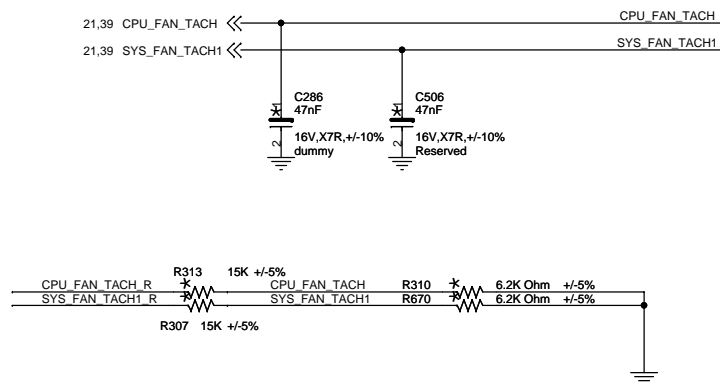
## SYS FAN



#### 4-pin FAN Header Definition

```
pin1. GND
pin2. +12V
pin3. Sense
pin4. Control
```

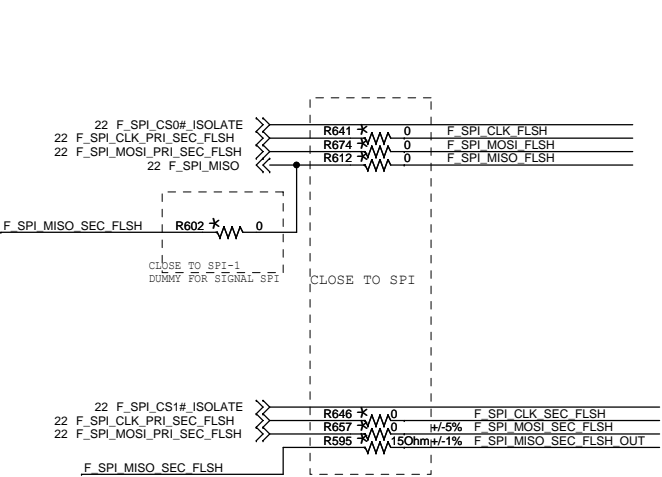
## FAN TACH



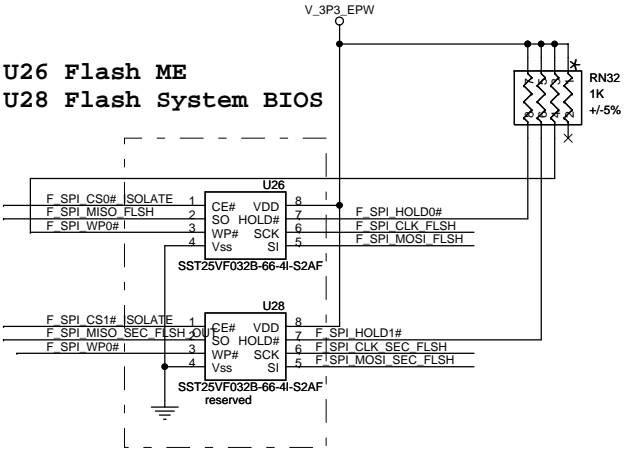
**FOXCONN PCEG**

Title				
<b>FAN</b>				
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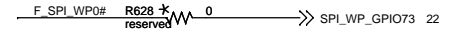
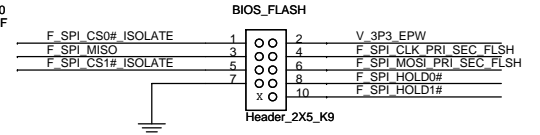
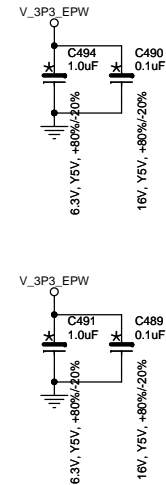
H55,H57 and Q57 SPI ROM size need 8MB for ME6.0 FW



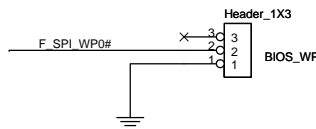
U26 Flash ME  
U28 Flash System BIOS



need to change to 64M SPI ROM



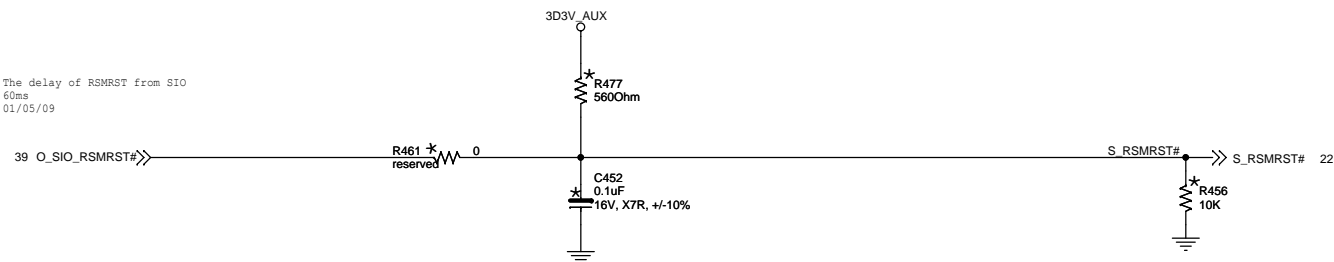
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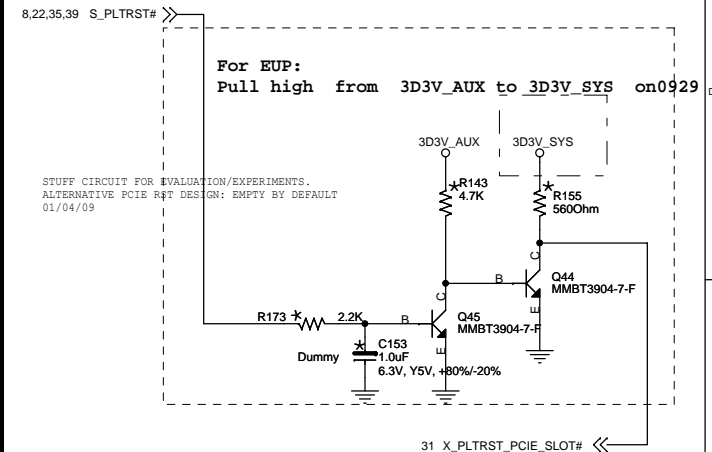
## RSMRST

The delay of RSMRST from SIO  
60ms  
01/05/09

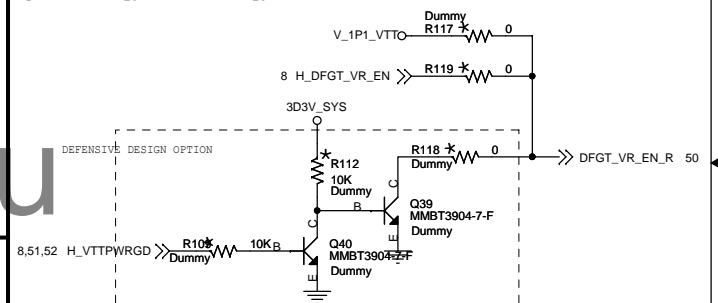


Ibex Peak SPEC:  
VccSUS active to RSMRST# inactive.  
T201>10ms.  
RSMRST# falling edge must transition  
to 0.8 V or less before VccSus3\_3  
drops to 2.85V.  
01/05/09

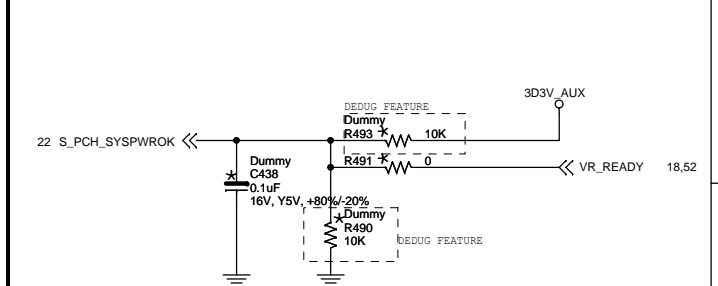
## PCI\_E1\_1X2 RESET



## GFX VR ENABLE DEFENSIVE



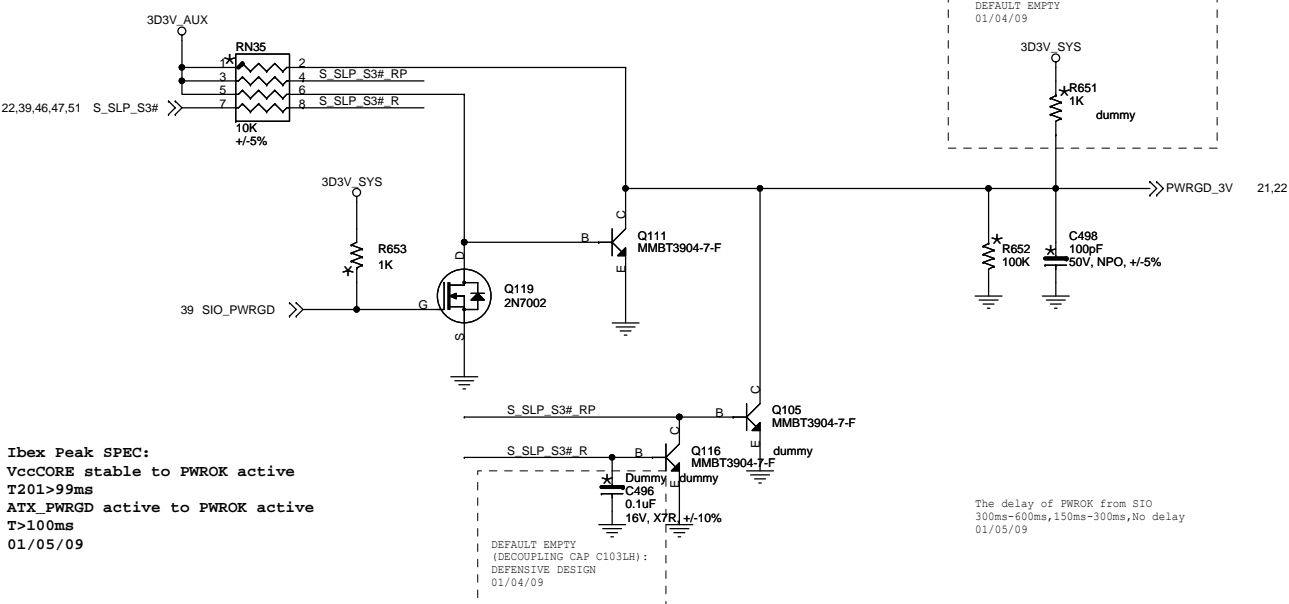
## VR\_READY DEFENSIVE (PCH POWEROK)



**FOXCONN**  
FOXCONN PCEG

POWER SEQUENCE		
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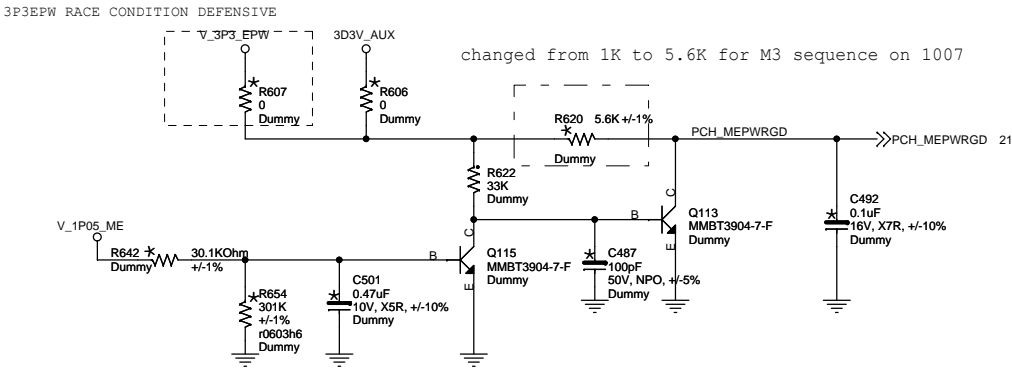
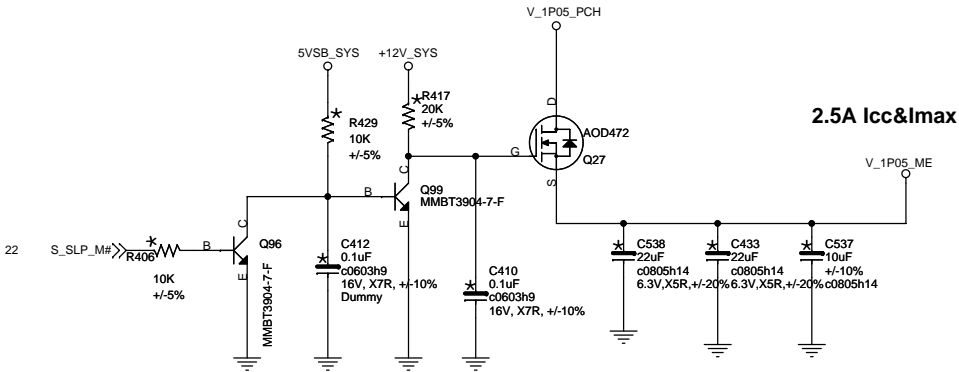
## POWER-GOOD 3V



Ibex Peak SPEC:  
VccCORE stable to PWROK active  
T201>99ms  
ATX\_PWROK active to PWROK active  
T>100ms  
01/05/09

V\_1P05\_ME

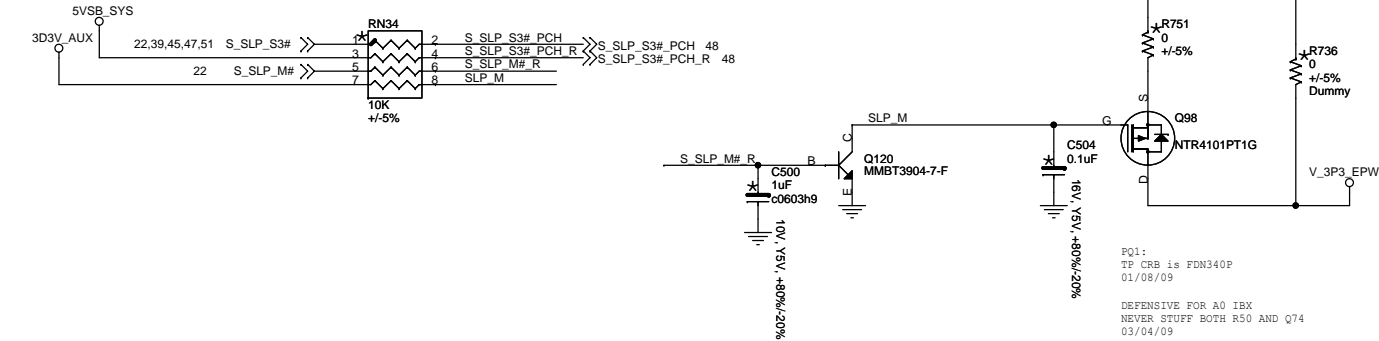
For Non-M3 support directly unstuff



- For Non-M3 support with third-party LAN:
- 1.delete V\_1P05\_ME power,directly connect it to V\_1P05\_PCH
  - 2.directly connect 3D3V\_SYS to V\_3P3\_EPW
  - 3.VCCLAN directly connect to GND
  - 4.LAN\_RST# connect to GND through restor
  - 5.MEPWRGD connect to PWRGD\_3V

V\_3P3\_EPW(FOR PCH ME)

For Non-M3 support, directly connect 3D3V\_SYS to V\_3P3\_EPW  
DEFENSIVE DESIGN: 3.3VPEW SUPPLY CONTROL  
03/04/09



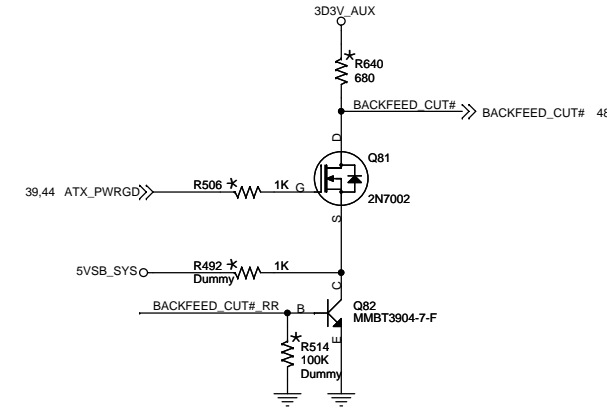
PQ1:  
TP CRB is FDN340P  
01/08/09  
DEFENSIVE FOR A0 IBX  
NEVER STUFF BOTH R50 AND Q74  
03/04/09



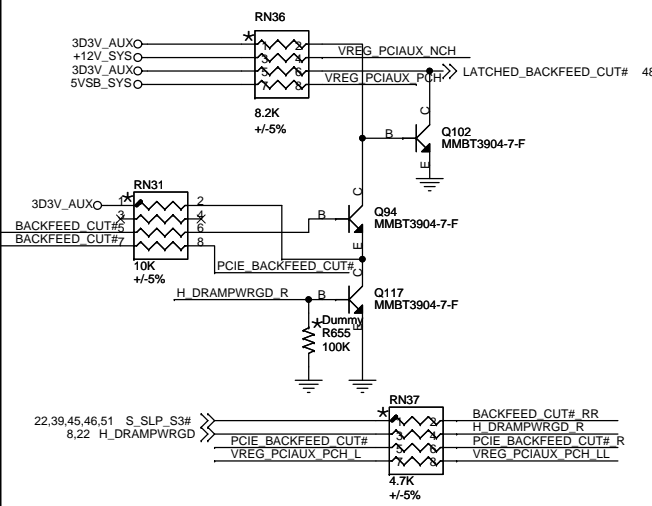
FOXCONN PCEG

Title		ME POWER
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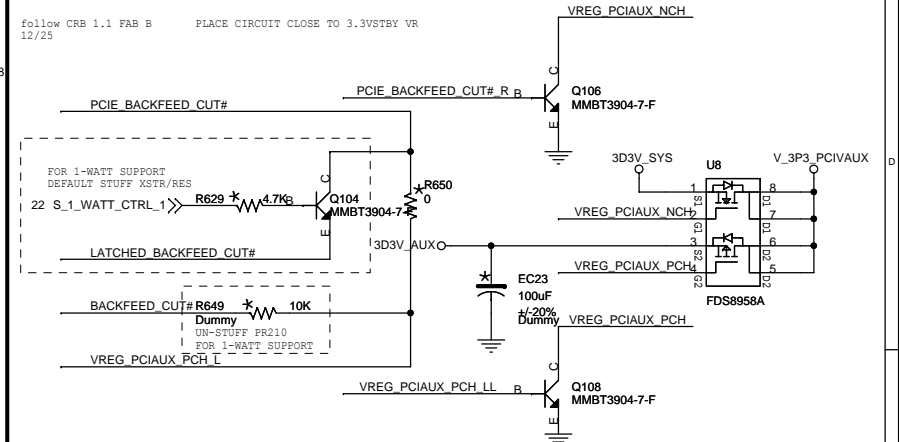
BACKFEED CUT



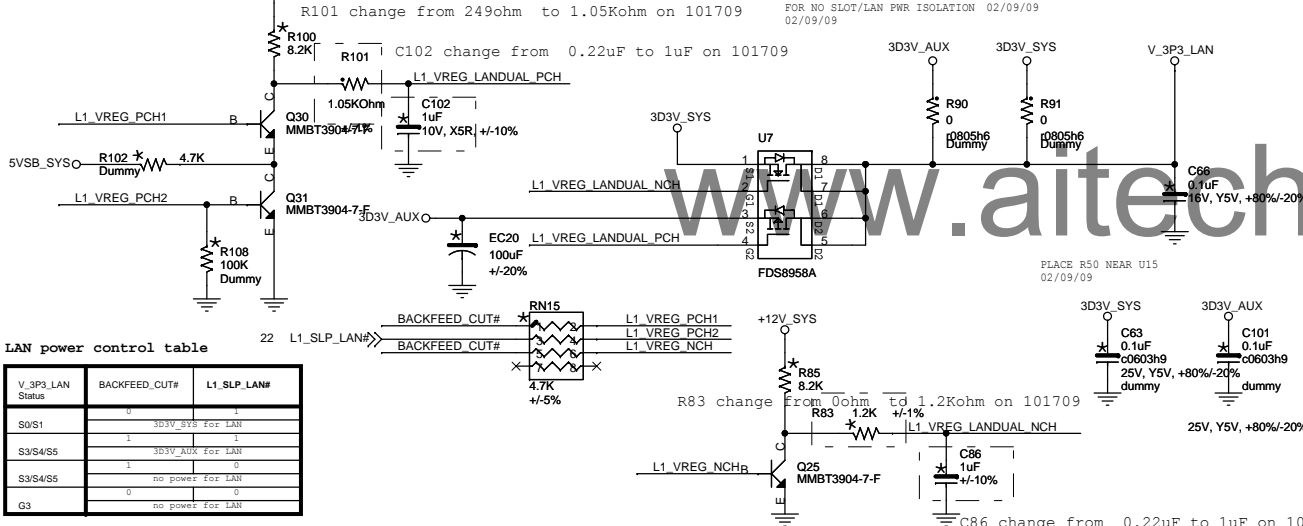
LATCHED BACKFEED CUT



V\_3P3\_PCIVAU (FOR PCI/PCIE SLOT)



LAN POWER



LAN power control table

V_3P3_LAN Status	BACKFEED_CUT#	L1_SLP_LAN#
S0/S1	0	1
S3/S4/S5	1	0
G3	0	0

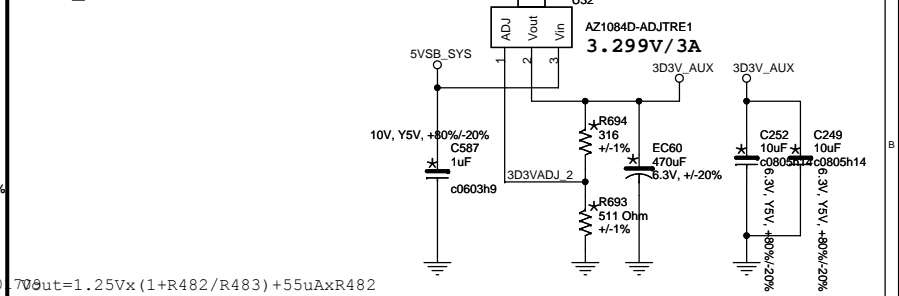
PCI-E SLOT power control table for 1-WATT support

V_3P3_PCIVAU Status	BACKFEED_CUT#	LATCHED_BACKFEED_CUT#	S_1_WATT_CTRL_1
S0/S1	0	0	0
S3	1	1	1/0
S4	1	1	0
S4	0	0	1
S5	1	0	0
S5	0	0	1
G3	0	0	0

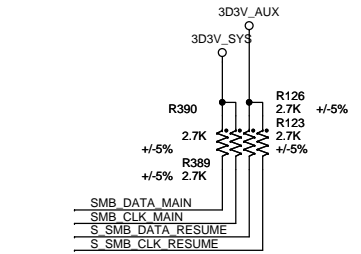
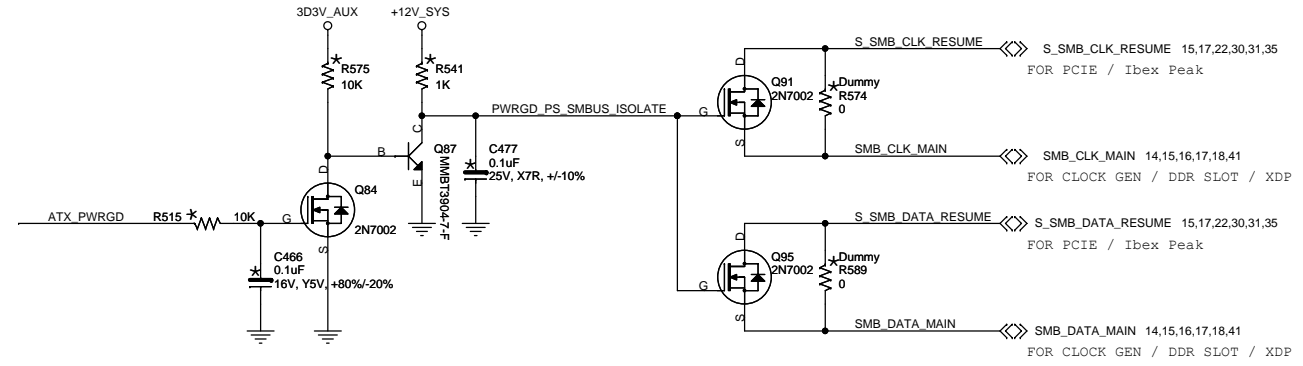
PCI-E SLOT power control table for none 1-WATT support

V_3P3_PCIVAU Status	BACKFEED_CUT#	LATCHED_BACKFEED_CUT#
S0/S1	0	0
S3	1	1
S4	1	0
S5	0	0
G3	0	0

3D3V\_AUX



SMB ISOLATE

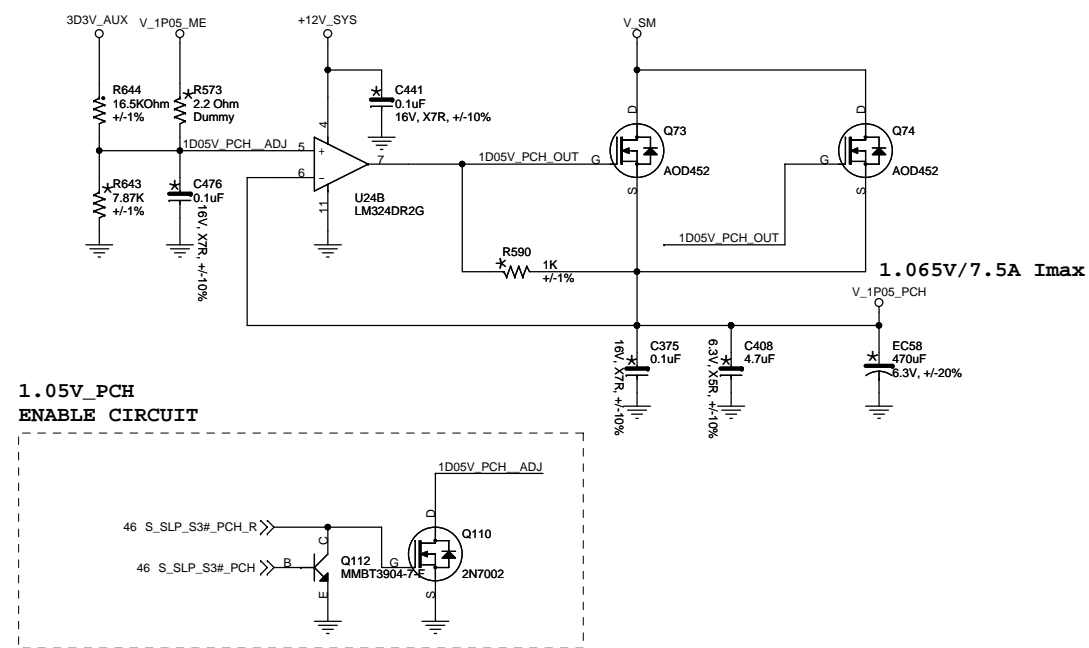


Title: POWER-1:LINEAR POWER-1

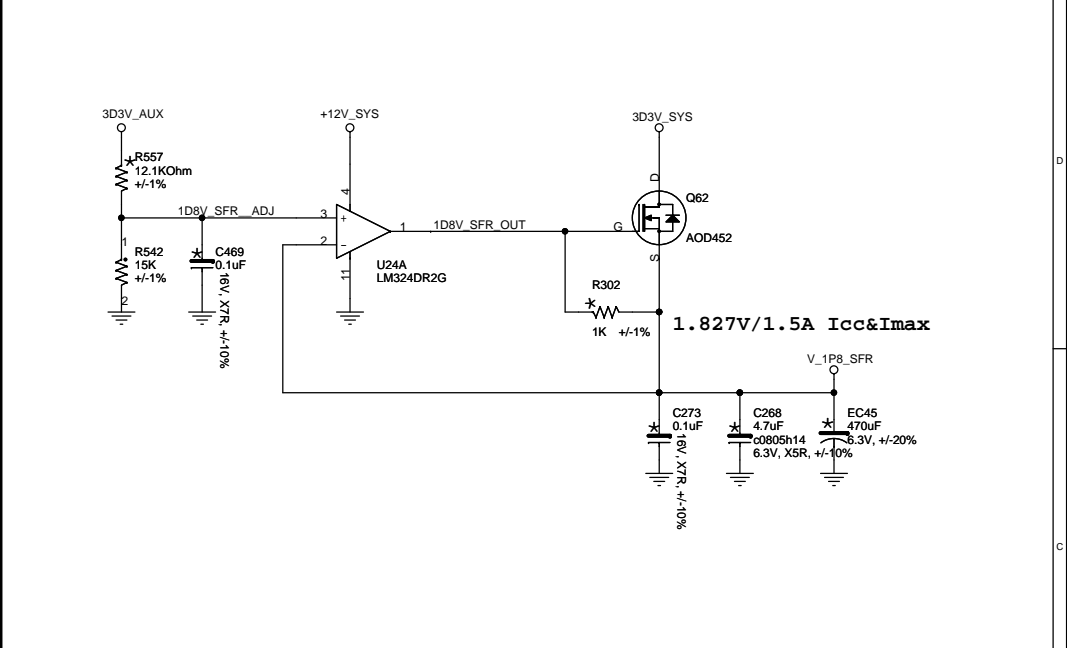
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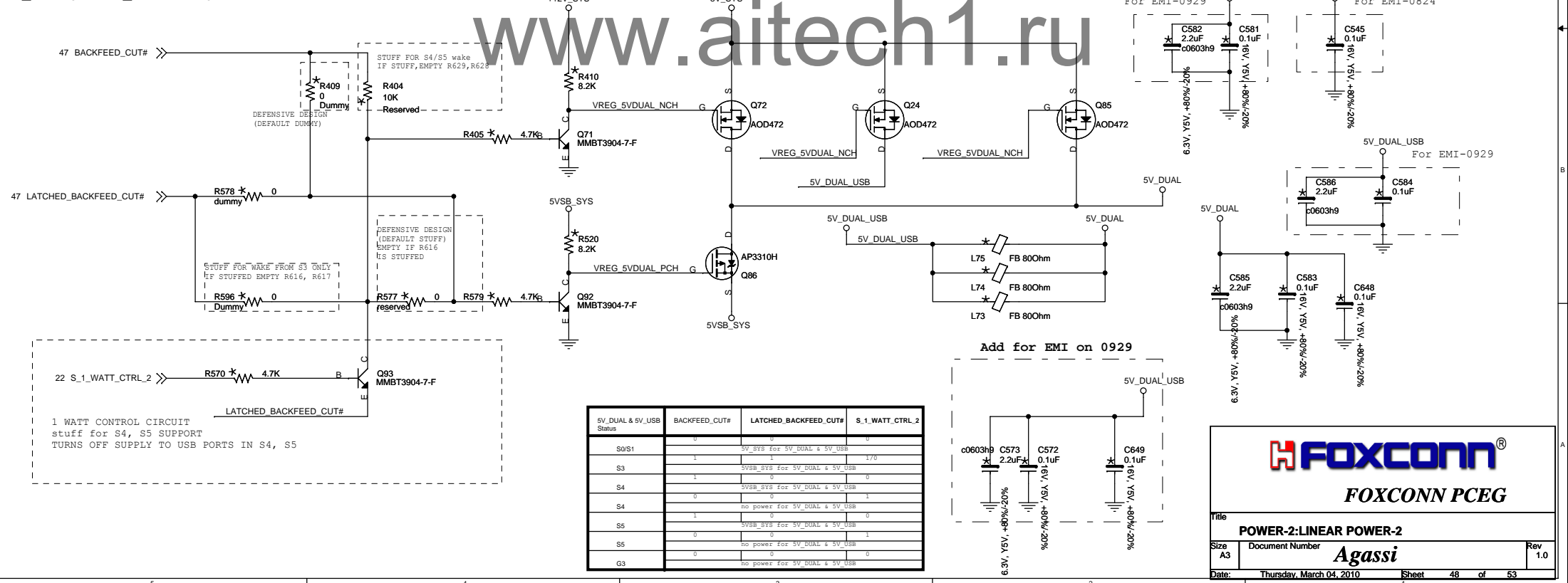
V\_1P05\_PCH



V\_1P8\_SFR



5V\_DUAL(For V\_SM/KBVCC)



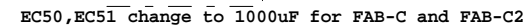
**FOXCONN PCEG**

Title: **POWER-2:LINEAR POWER-2**

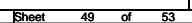
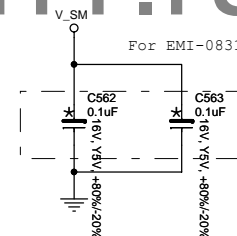
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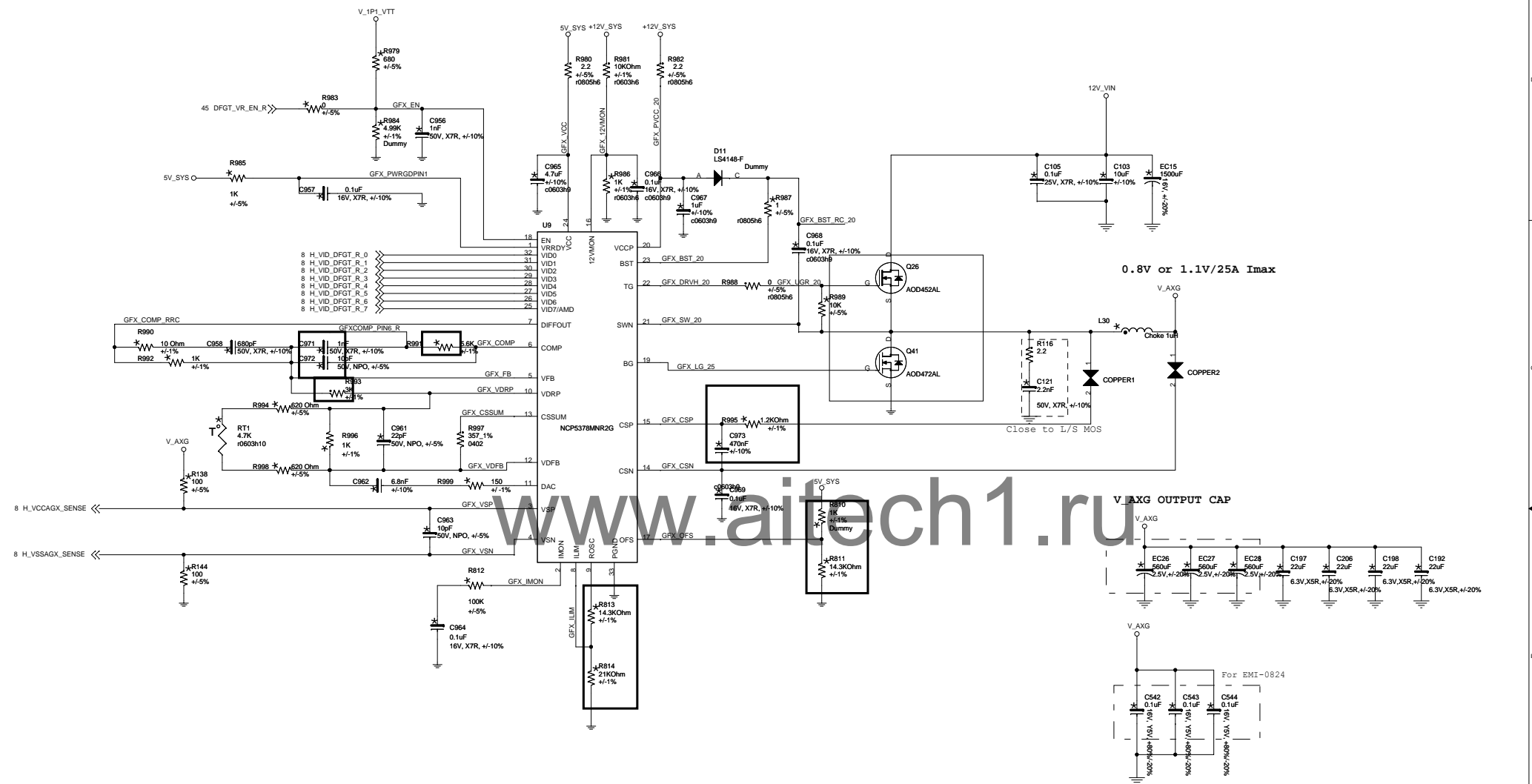
1.50V/25A I<sub>max</sub>



dummy  
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VAXG(1.1V)



```
| MLCG 220P + 20T - - - - -
```

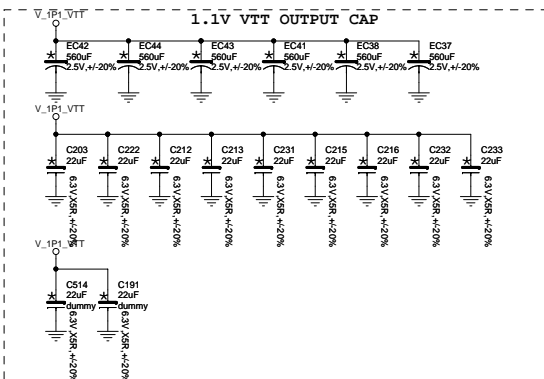
| 5pcs in the southeast corner of the socket cavity,  
| 4pcs in the west side of socket  
| 01/08/09

| Aluminum Polymer

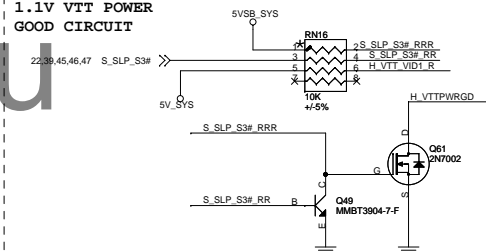
| 5pcs East side by the output of the VR  
| 1pcs West side of the socket  
| 01/08/09

| 1pcs MLCG(dummy)C11VR PLACED ON BACKSIDE OF THE BOARD  
| 01/08/09

Input LC circuit

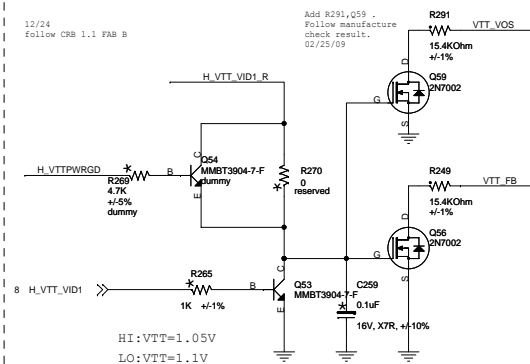


```
| 1.1V VTT POWER
| GOOD CIRCUIT
```



12/24  
follow CRB 1.1 FAB B

Add R291,Q59  
Follow manufa  
check result.  
02/25/09



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POWER-5:VTT			
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18.45 VR\_READY  
8.45.51 H\_VTTPWRGD  
8 H\_VID\_ISOLATE0  
8 H\_VID\_ISOLATE1  
8 H\_VID\_ISOLATE2  
8 H\_VID\_ISOLATE3  
8 H\_VID\_ISOLATE4  
8 H\_VID\_ISOLATE5  
8 H\_VID\_ISOLATE6  
8 H\_VID\_ISOLATE7  
8 H\_MCP\_PSI#

34 VR\_RDY  
33 EN  
32 VID0  
31 VID1  
30 VID2  
29 VID3  
28 VID4  
27 VID5  
26 VID6  
25 VID7  
24 PSI  
23 DIFFOUT

17 COMP  
16 VFB  
15 DROOP  
14 VDFB  
13 CSSUM  
12 DAC  
11 VSP  
10 VSN

8 H\_VCC\_SENSE  
8 H\_VSS\_SENSE

12 VRM\_GND  
11 VRM\_GND  
10 VRM\_GND  
9 VRM\_GND  
8 VRM\_GND  
7 VRM\_GND  
6 VRM\_GND  
5 VRM\_GND  
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12 VRM\_GND  
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12 VRM\_GND  
11 VRM\_GND  
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6 VRM\_GND  
5 VRM\_GND  
4 VRM\_GND  
3 VRM\_GND  
2 VRM\_GND  
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12 VRM\_GND  
11 VRM\_GND  
10 VRM\_GND  
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5 VRM\_GND  
4 VRM\_GND  
3 VRM\_GND  
2 VRM\_GND  
1 VRM\_GND

12 VRM\_GND  
11 VRM\_GND  
10 VRM\_GND  
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8 VRM\_GND  
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5 VRM\_GND  
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3 VRM\_GND  
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1 VRM\_GND

12 VRM\_GND  
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8 VRM\_GND  
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7 VRM\_GND  
6 VRM\_GND  
5 VRM\_GND  
4 VRM\_GND  
3 VRM\_GND  
2 VRM\_GND  
1 VRM\_GND

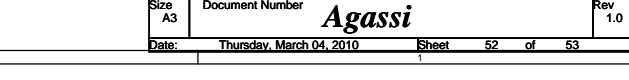
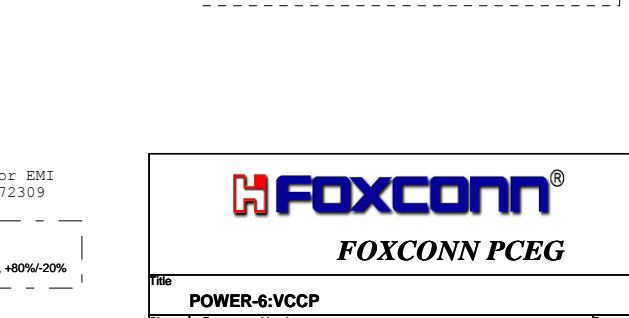
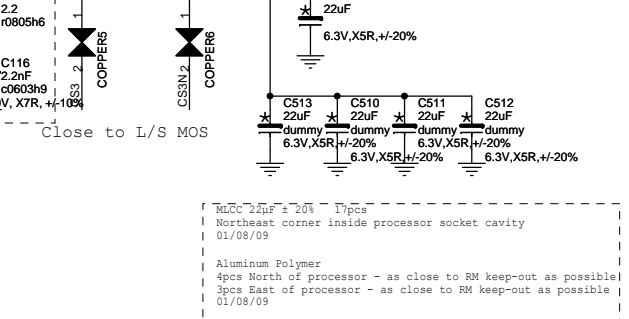
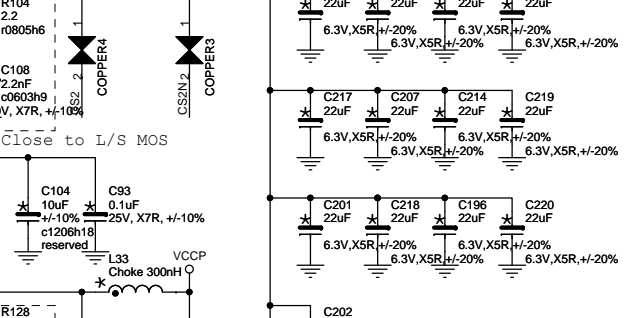
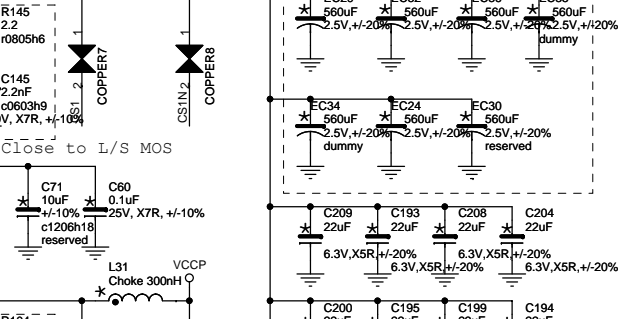
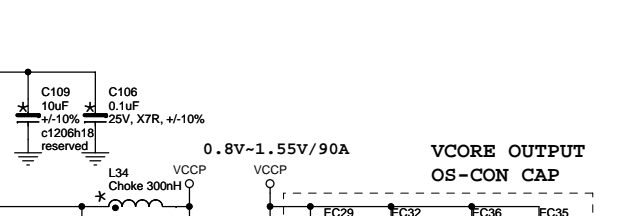
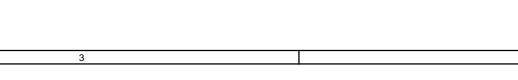
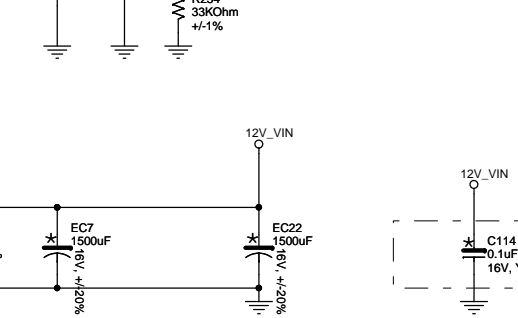
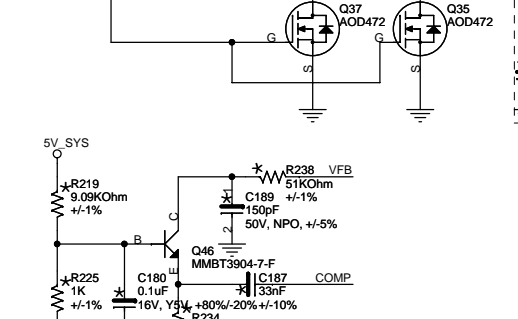
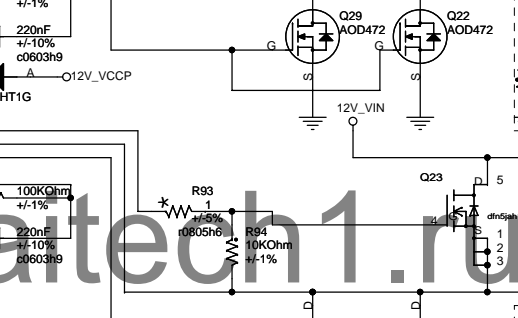
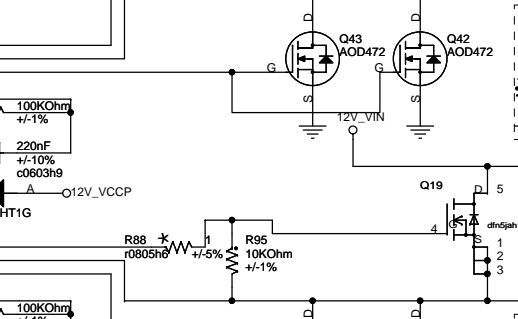
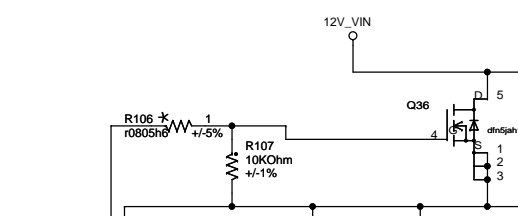
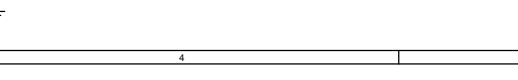
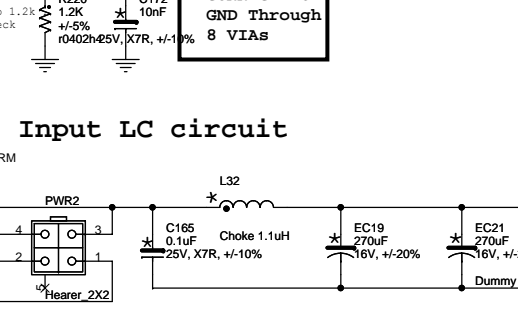
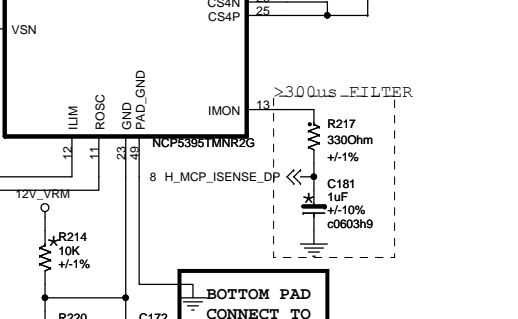
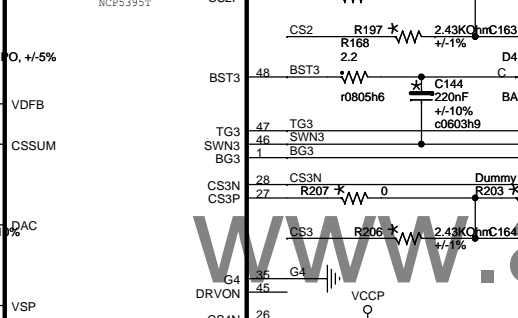
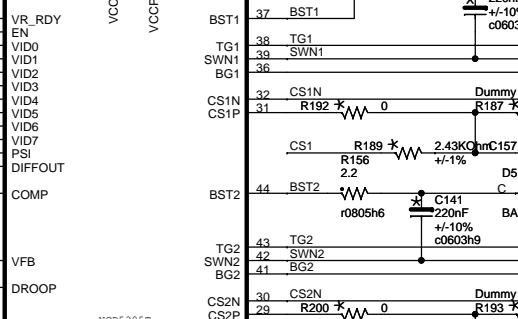
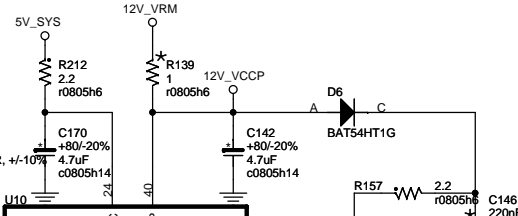
12 VRM\_GND  
11 VRM\_GND  
10 VRM\_GND  
9 VRM\_GND  
8 VRM\_GND  
7 VRM\_GND  
6 VRM\_GND  
5 VRM\_GND  
4 VRM\_GND  
3 VRM\_GND  
2 VRM\_GND  
1 VRM\_GND

12 VRM\_GND  
11 VRM\_GND  
10 VRM\_GND  
9 VRM\_GND  
8 VRM\_GND  
7 VRM\_GND  
6 VRM\_GND  
5 VRM\_GND  
4 VRM\_GND  
3 VRM\_GND  
2 VRM\_GND  
1 VRM\_GND

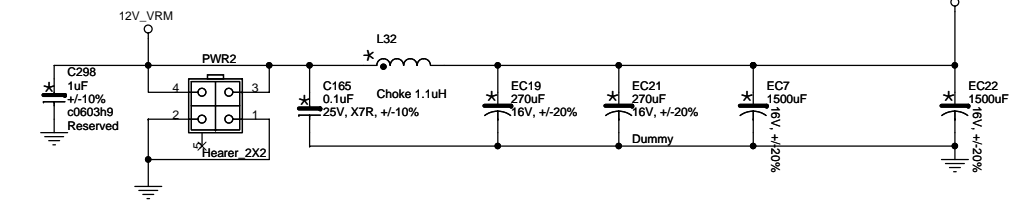
12 VRM\_GND  
11 VRM\_GND  
10 VRM\_GND  
9 VRM\_GND  
8 VRM\_GND  
7 VRM\_GND  
6 VRM\_GND  
5 VRM\_GND  
4 VRM\_GND  
3 VRM\_GND  
2 VRM\_GND  
1 VRM\_GND

12 VRM\_GND  
11 VRM\_GND  
10 VRM\_GND  
9 VRM\_GND  
8 VRM\_GND  
7 VRM\_GND  
6 VRM\_GND  
5 VRM\_GND  
4 VRM\_GND  
3 VRM\_GND  
2 VRM\_GND  
1 VRM\_GND

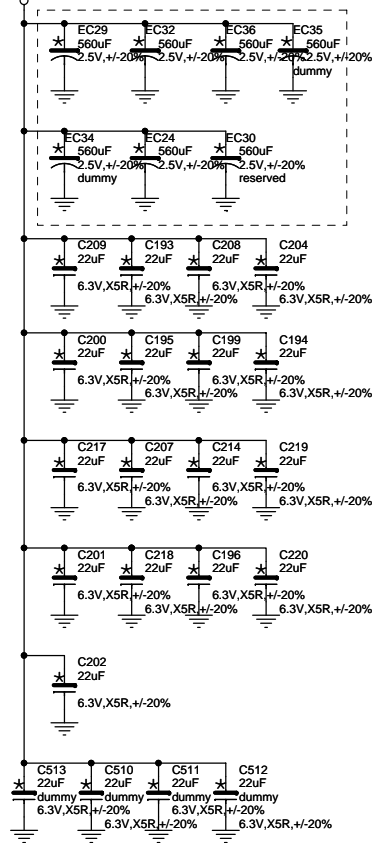
12 VRM\_GND  
11 VRM\_GND  
10 VRM\_GND  
9 VRM\_GND  
8 VRM\_GND  
7 VRM\_GND  
6 VRM\_GND  
5 VRM\_GND  
4 VRM\_GND  
3 VRM\_GND  
2 VRM\_GND  
1 VRM\_GND



Input LC circuit

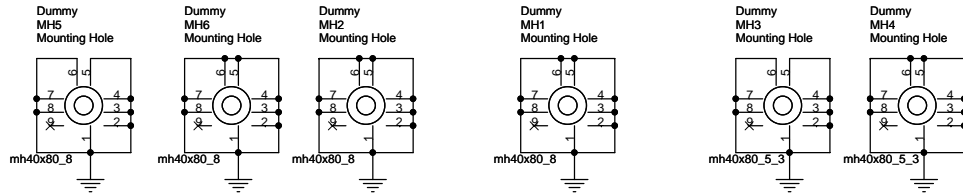
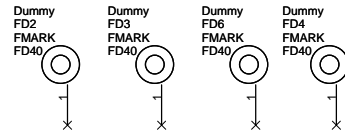
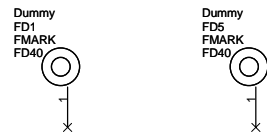


VCORE OUTPUT OS-CON CAP

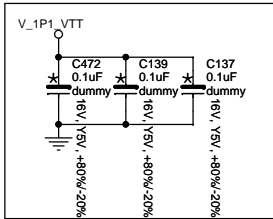


1uF, +/-20%  
Northeast corner inside processor socket cavity  
01/08/09  
Aluminum Polymer  
4pcs North of processor - as close to RM keep-out as possible  
3pcs East of processor - as close to RM keep-out as possible  
01/08/09

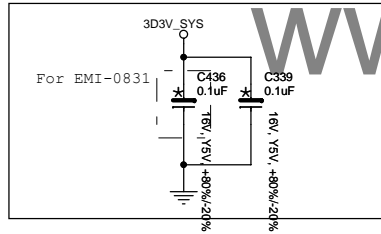
FOXCONN  
FOXCONN PCEG  
Title  
POWER-6:VCCP  
Size A3  
Document Number  
Agassi  
Date  
Thursday, March 04, 2010  
Sheet 52 of 53  
Rev 1.0



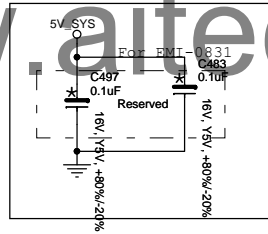
Stitch for DMI reference plane



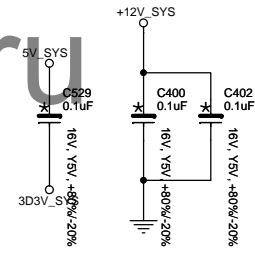
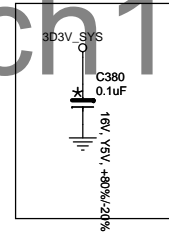
Stitch for 96M clock reference plane



Stitch for LAN PCIE/Clock difference reference plane



Stitch for PCICLK



FOXCONN PCEG

Title		EMI
Size	Document Number	Agassi
A3		Rev 1.0
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